SMD I²C Pyroelectric Infrared Sensor

Reference Manual

Single Element or 2x2 Array

QFS Flame Sensors

QGS Gas Sensors

QMS Motion & Gesture Sensors

Rev. 1.2

SEP 2020

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1 INTRODUCTION

KEMET's range of thin film digital pyroelectric IR USEQ*S sensors combines high performance with a high level of configurable electronic integration in the smallest SMD package. High sensitivity and SNR combined with fast response times ensure rapid and accurate detection. High dynamic range allows motion and flame detection nearby or over larger distances. Programmable gain and filtering offer maximum flexibility, while industry standard I^2C I/O enables plug-and-play connectivity to microcontrollers and easy tuning. These sensors can also be daisy-chained to allow synchronized sampling across devices and offer various low power modes, including a wake-up by motion feature. The 2x2 pixel version of this device allows users to determine direction of motion.

2 DEVICE PARAMETERS

Table 1 - Preliminary

Parameter	Conditions	Minimum	Typical	Maximum	Unit
D* – Single Pixel	10 Hz, 500 K, 25°C		2.5 x 10^{8} [1]		$cm\sqrt{Hz}/W$
NEP – Single Pixel	10 Hz, 500 K, 25°C		2.7 x 10^{-10} [1]		$W/\sqrt{Hz}$
D* – 2x2 Array	10 Hz, 500 K, 25°C		5.5 x 10^{8} [1]		$cm\sqrt{Hz}/W$
NEP – 2x2 Array	10 Hz, 500 K, 25°C		0.4 x 10^{-10} [1]		$W/\sqrt{Hz}$
Package Dimensions			5.65 x 3.7 x 1.35	h = 1.55	mm
Pixel Area – Single Pixel			1 px at 0.64 x 0.64		mm
Pixel Area – 2x2 Array			4 px at 0.057		mm^2
Aperture – Small Option			ø 0.9		mm
Aperture – Large Option			ø 1.65		mm
FoV – Large Aperture			90°	117°	
Operating Temperature		-40		85	°C
Storage Temperature		-40		110	°C
Supply Voltage		1.75		3.6	V
Supply Current	Room Temperature		1.1 to 65		µA
I^2C Communication Rate	Fast Mode Plus (FM+)			1	MHz

[1] No optical filter, 10 Hz optical chopper frequency, 500 K blackbody source temperature, room temperature – for typical values with part-specific optical filters see Section 5.

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3 ORDERING INFORMATION

Table 2 – Product Types

Part Number	Pixels	Aperture (ø)	Optical Filter	Application
Broad Infrared Range				
USEQFSEA22L180	1	L – 1.65 mm	2.20 µm Long-Pass	2.5-6 µm Broadband
USEQFSEA50L180	1	L – 1.65 mm	5.0 µm Long-Pass	6-14 µm Broadband, Human Motion
USEQMSEA011680	1	L – 1.65 mm	5.0 µm Long-Pass	Motion
USEQMSEA221680	2x2	L – 1.65 mm	5.0 µm Long-Pass	Motion and Direction, Gesture
USEQMSEA220980	2x2	S – 0.9 mm	5.0 µm Long-Pass	Gesture
Narrow Infrared Band				
USEQFSEA391180	1	L – 1.65 mm	CWL = 3.91 µm, FWHM = 90 nm	Reference (Gas), Flame Rejection
USEQGSEACH4180	1	L – 1.65 mm	CWL = 3.30 µm, FWHM = 160 nm	CH_4 Gas
USEQGSEAC82180	1	L – 1.65 mm	CWL = 4.26 µm, FWHM = 180 nm	CO_2 Gas
USEQFSEA464180	1	L – 1.65 mm	CWL = 4.64 µm, FWHM = 180 nm	CO Gas, Flame
USEQFSEA448180	1	L – 1.65 mm	CWL = 4.48 µm, FWHM = 620 nm	Flame
USEQGSEAN8L180	1	L – 1.65 mm	CWL = 5.30 µm, FWHM = 180 nm	NO gas

Narrow band infrared filters blocking up to 8 µm or higher: blocking filter should be added above the sensor.

CWL: Centre Wavelength (Nominal filter value per Figure 1).

FWHM: Full Width Half Maximum (Cut on to Cut off per Figure 1).

Long-Pass: Passes radiation above given wavelength.

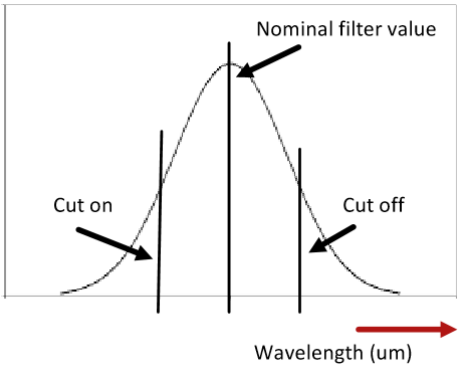

Figure 1 – Narrow Band Infrared Filter Diagram

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4 TYPICAL INFRARED CHARACTERISTICS

4.1 Infrared Signal and Noise

Table 3 – Signal and Noise Measurements

Part Number	Typical Signal Measurement (ADC counts RMS)	Typical Noise Measurement (ADC counts RMS)
USEQFSEA22L180	24,500	TBA
USEQFSEA50L180	10,500	85
USEQMSEA011680	10,500	85
USEQMSEA221680	850	5.5
USEQMSEA220980	760	5.5
USEQFSEA391180	1,050	85
USEQGSEACH4180	405	85
USEQGSEAC82180	2,450	85
USEQFSEA464180	2,150	85
USEQFSEA448180	6,600	85
USEQGSEAN8L180	1,900	85

4.1.1 Measurement Conditions

Infrared signal given in the Typical Infrared Characteristics section is measured under the following conditions:

- Pulsed infrared emitter operating at 10 Hz rate
- SMD sensor settings: low gain (3,200 fF), wide signal filtering (HPF = 1 Hz, LPF = 180 Hz), low transconductance (0.15 TΩ)

Noise is measured with the emitter switched off.

4.2 Frequency Response

Characteristic frequency response plots are shown in Figures 2 to 5.

The measurements are obtained using a blackbody source set to temperature of 500 K, with a variable frequency optical chopper.

The plots are normalised per figure and show general USEQ*S frequency characteristics across the product range.

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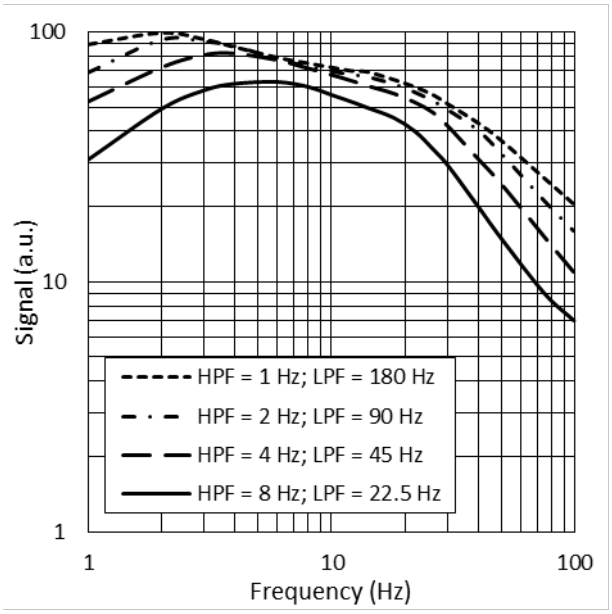

Figure 2 – Typical Frequency Response in Normal Power Mode – Signal Filtering Effect (Transconductance = 1.2 TΩ, Gain = 400 fF)

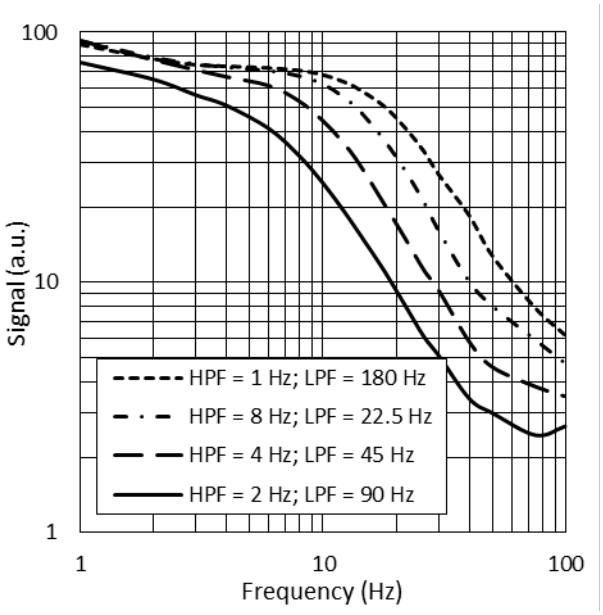

Figure 3 – Typical Frequency Response in Low Power Mode – Signal Filtering Effect (Transconductance = 1.2 TΩ, Gain = 400 fF)

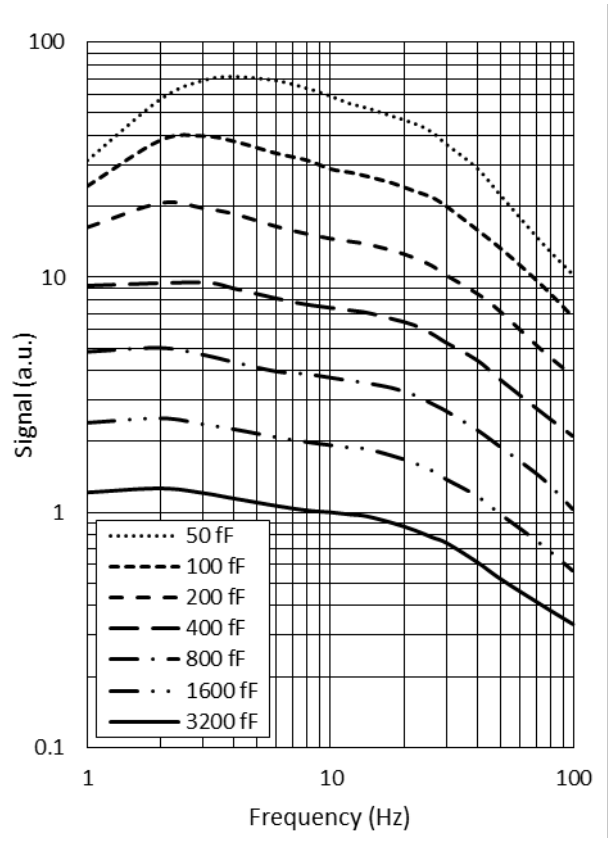

Figure 4 – Typical Frequency Response Gain Effect (Normal Power Mode, HPF = 1 Hz, LPF = 180 Hz, Transconductance = 1.2 TΩ)

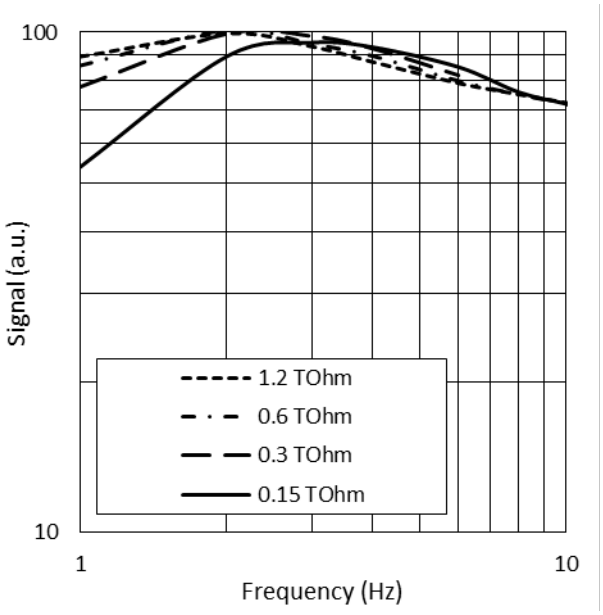

Figure 5 – Typical Frequency Response Transconductance Effect (Normal Power Mode, HPF = 1 Hz, LPF = 180 Hz, Gain = 400 fF)

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5 ABSOLUTE MAXIMUM RATINGS

Table 4

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{Supply}		3.6	V
Digital Inputs		-0.3	V_{Supply} + 0.3	V
Storage Temperature		-40	110	°C
Operating Temperature		-40	85	°C

6 ELECTRICAL CHARACTERISTICS

6.1 Power Supply

Table 5

Parameter	Conditions	Typical	Unit
Supply Voltage		1.75 – 3.6	V
Supply Current V_{Supply} = 1.8 V, T_A = 27°C	Power Down Mode (CS = 0 V)	1.1	µA
	Normal Power Mode, 4 active channels at 1 ksps	61	µA
	Normal Power Mode, 1 active channel at 1 ksps	22	µA
	Sleep Mode in Normal Power Mode	21	µA
	Low Power Mode, 4 active channels at 166 sps	7.5	µA
	Low Power Mode, 1 active channel at 166 sps	3.5	µA
	Sleep Mode in Low Power Mode	3.5	µA
Supply Current V_{Supply} = 3.3 V, T_A = 27°C	Power Down Mode (CS = 0 V)	2	µA
	Normal Power Mode, 4 active channels at 1 ksps	65	µA
	Normal Power Mode, 1 active channel at 1 ksps	23	µA
	Sleep Mode in Normal Power Mode	21	µA
	Low Power Mode, 4 active channels at 166 sps	9	µA
	Low Power Mode, 1 active channel at 166 sps	4.5	µA
	Sleep Mode in Low Power Mode	4.5	µA

- 1 ksps = 1 kHz sampling rate; 166 sps = 166 Hz sampling rate
- 1 active channel applies to single pixel devices
- 4 active channels apply to full operation of 2x2 array devices

Typical current consumption increments for every enabled channel:

- approximately 1.35 µA in Low Power Mode
- approximately 13 µA in Normal Power Mode

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7 PINOUT

7.1 Pin Configuration

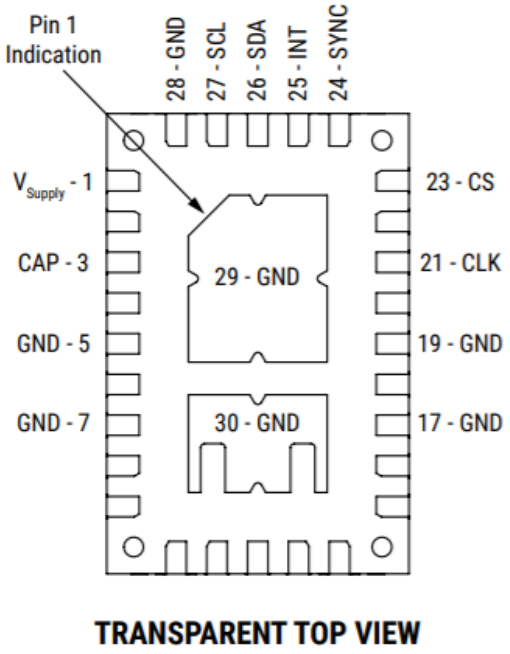

Figure 6 – Pin Configuration

7.2 Pin Descriptions

Table 6

Pin	Symbol	Type	Description
1	V_{Supply}	Power Supply	Power supply
3	CAP	Power Supply	100 nF capacitor (minimum) connected to ground
5, 7, 17, 19, 28, 29, 30	GND	Ground	Package and circuit ground
21	CLK	Digital In/Out	**Optional:** multiple USEQ*S package synchronisation (default Out)
23	CS	Digital In	**Chip Select:** can be controlled by MCU or connected to V_{Supply}[2] **Important:** see section 12.8 for power up sequence
24	SYNC	Digital In/Out	**Optional:** multiple USEQ*S package synchronisation (active low, default Out)
25	INT	Digital Out	**Optional:** interrupt output (active low); set whenever there is data in the FIFO buffer (Normal Operation Mode) or an infrared event occurs (Sleep Mode)
26	SDA	Digital In/Out	**I^2C:** data line (pull-up resistor required)
37	SCL	Digital In	**I^2C:** clock line (pull-up resistor required)

[2] For multiple devices on I^2C bus when CS is connected to V_{Supply}, power needs to be switchable in order to allow individual I^2C address programming on power up.

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8 BLOCK DIAGRAM

Sensor elements connected to readout channels as per section 11.2.

8.1 Sensor with 2x2 Array

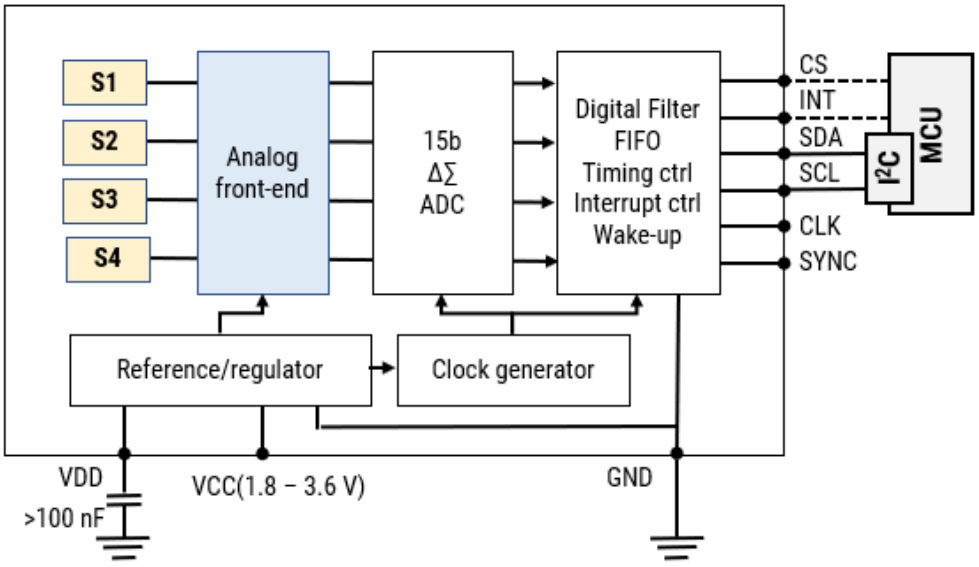

*Figure 7 – Block Diagram – USEQ*S Sensor with 2x2 Array*

8.2 Sensor with Single Element

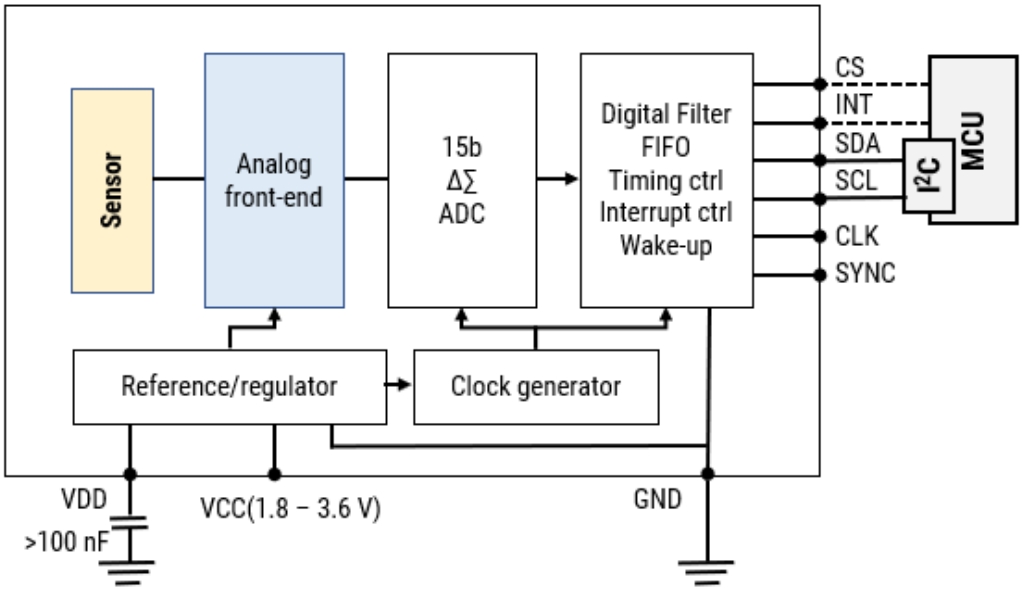

*Figure 8 – Block Diagram – USEQ*S Sensor with Single Element*

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9 MECHANICAL

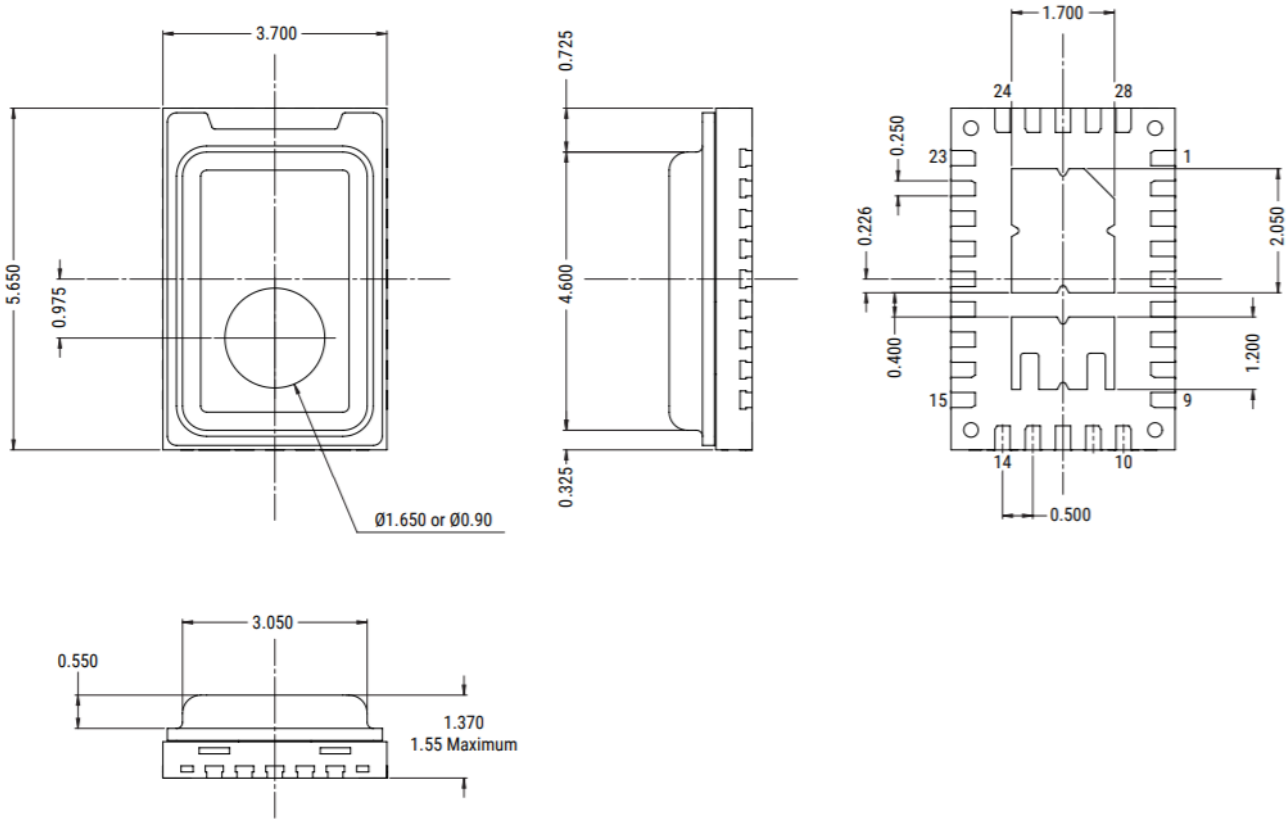

Figure 9 – Dimensions - Millimeters

Materials: Custom AQFN moulded package base with metal lid.

Drawing subject to change without further notification.

10 PACKAGE MARKING

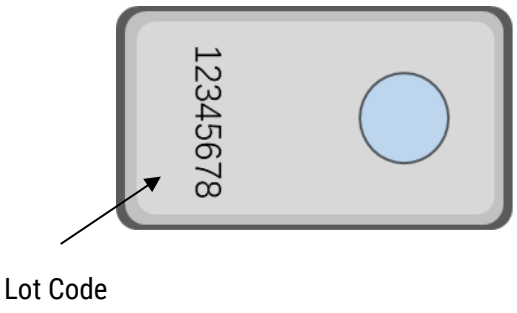

Figure 10 – Package Marking

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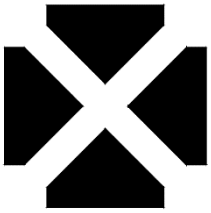
11 SENSOR ELEMENT LAYOUT

11.1 Sensor Elements

Single Element

1 pixel
0.64 mm x 0.64 mm

2x2 Array

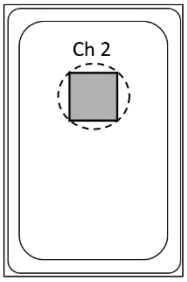


4 pixels
approx. triangle a = 0.420 mm h = 0.250 mm

Figure 11 – Sensor Element Layout

11.2 Pixel Mapping

Single Element



2x2 Array

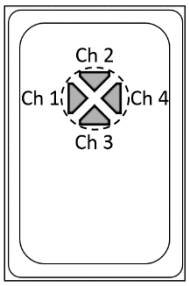
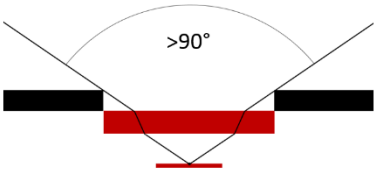


Figure 12 – Pixel Mapping

Channel 0 is currently used for test purposes only.

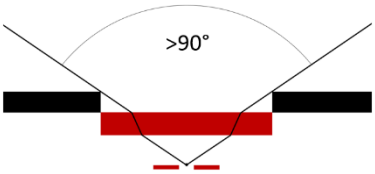
11.3 Field of View

Single Element



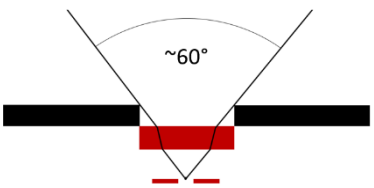
Large Aperture

2x2 Array



Large Aperture

2x2 Array



Small Aperture

Figure 13 – Field of View

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12 FEATURES

12.1 Power Management

The power management modes that the sensor can be configured to are listed in Table 7. Apart from global power mode, each channel can be enabled/disabled independently to optimise power consumption of the sensor as needed in an application.

In the Low Power Mode, the power required for each channel is reduced by 6-8 times and the maximum sampling rate drops from 1 kHz to 166 Hz. Signal filtering is also shifted to lower frequencies by a factor of 6.

Sleep Mode can be entered while either in Normal Power Mode or Low Power Mode.

Table 7 – Power Modes

	Mode	Description
Power Consumption	Normal Power Mode	Normal power consumption, 1 kHz max. sample rate
	Low Power Mode	Low power consumption, 166 Hz max. sample rate
Operational State	Normal Operation Mode	Sensor signal readout over I^2C
	Sleep Mode	Hardware interrupt on infrared trigger
	Power Down Mode	Sensor is disabled
Channel States	Channel Status	Each channel can be enabled or disabled

Sleep Mode operation is described in section 12.7.4. Power Down Mode is selected by disabling CS pin. Normal and Low Power Mode switching is part of analog front-end packet (AFEP) explained in section 13.3.6.

Selection of a Normal Power Mode or Low Power Mode affects power consumption, maximum sampling rate, as well as signal filtering time constants.

12.2 Sensor Signal Processing

12.2.1 Signal Filtering

Signal processing capabilities of USEQ*S sensors mean that each sensor can be adapted to the needs of a specific application. The power mode selected affects effective cut-on and cut-off frequencies as illustrated in Table 8. The measured infrared frequency characteristics are illustrated in Figures 2 to 5 of section 4.2.

Figure 14 – Signal Processing Block Diagram

Table 8 – Signal Filtering Settings

Power Mode (base sample rate)	High Pass Filter – Analog (Hz)					Fixed Analog Low Pass Filter (Hz)	Fixed Digital Low Pass Filter (Hz)	Digital Low Pass Filter (Hz)				Max ADC Sampling Rate (sps)
Normal Power Mode	Off	1	2	4	8	600	250	180	90	45	22.5	1,000
Low Power Mode	Off	0.17	0.33	0.66	1.3	100	42	30	15	7.5	3.75	166
Setting Command Value		00	01	10	11	N/A	N/A	00	01	10	11	

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12.2.2 Saturation Handling

Sometimes the sensor readout channel can be saturated due to excessive incident infrared radiation or a strong thermal shock. With a very slow high pass filter the recovery time from saturation may take many seconds while the sensor signal returns into the operating region. During this period the sensor signal is not useable for analysis. A fast reset circuit is implemented within the readout circuit to accelerate this recovery time.

The fast reset will act as following:

- Once the fast reset is ended, the circuit will resume their previous setting.
- When the output of the amplifier is saturated or the ADC is outside of 6.25% - 93.7% of the full-scale value for a minimum 4 ms, the fast reset circuit is enabled for 40 ms after the saturation event ends.
- When the reset is active, the 23rd bit of the data packet is also set to indicate a reset action is ongoing.
- The fast reset is also active for 40 ms after any channel is re-enabled. This improves the start-up stabilisation time of the channel.

12.3 Interrupt Controller

The interrupt controller generates a hardware interrupt output when a sensor data frame is loaded into the FIFO buffer (Normal Operation Mode) or a wake-up event is detected (Sleep Mode).

Bit 0 in byte 1 of AFEP register controls the interrupt output. When it is set, the interrupt output is enabled. Default value is enabled (1). The interrupt is always enabled in Sleep Mode even when it was programmed as disabled.

In Normal Operation Mode, the INT signal is active (low) when the FIFO is not empty, and deactivated (high) when the FIFO is empty.

The readout procedure for interrupt and polling modes is described in section 12.6.1.

There is a delay (~100 µs in Normal Power Mode and 400 µs in Low Power Mode) between the I²C commands FIFO_READ_FULL/FIFO_READ_ACTIVE and the rising edge of the INT signal.

12.4 External Synchronization (Daisy-Chaining)

The sensor by default uses the internal clock generator for all timing. When multiple sensors are used in the same system, one IC can be configured as a sync master and the others as a sync slaves (in the timing context, not I²C).

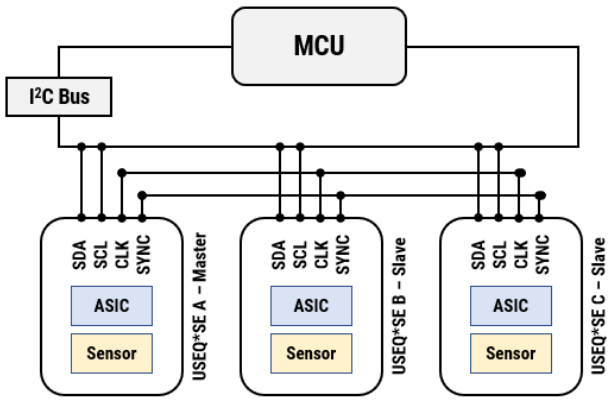

Figure 15 – Synchronisation Example - Three Devices with Synchronised Sampling

As illustrated in Figure 15, two pins are used for this purpose: CLK and SYNC.[3]

[3] SYNC pin is active low.

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- In the sync master mode (default) the CLK pin is an output pin of the internal clock generator, SYNC pin is also an output pin which allow the sync slave device to synchronize with the sync master.
- In sync slave mode, the internal clock generator is not used; CLK and SYNC pin become inputs.
- The SYNC pin on the sync master device outputs the synchronization signal for the sampling point (output rate). The output rate is controlled by bits [7:0] in AFEP on the sync master device.
- If on the rising edge of the CLK and SYNC is low, then the content of the accumulator is written into the FIFO and then reset to zero. In the sync slave device, the value of the S7-S0 in AFEP register has no effect.
- In case there are multiple sync masters in the configuration, or if there are only sync slaves, the system behaviour is undefined.

The sync master/slave mode is configured by bit SYNC in AFEP.

12.5 Sensor Data FIFO Buffer

A 14 position (frame) FIFO buffer is available with each position (frame) containing the ADC data from 5 sensor readout channels and a frame counter.

When a channel is inactive, its value within the frame is set to 0.

A FIFO_READ command reads the data packet of the FIFO associated with the current read pointer that is then freed and can be overwritten. A FIFO_CLEAR command also frees the currently addressed data packet.

A lock mechanism ensures that a frame record cannot be corrupted with new data until the complete record has been read. This only applies while a read operation is in progress and the FIFO is full, resulting in new data being discarded.

The filtered ADC data is 15 bits unsigned data. After accumulating up to 256 samples, it is 23 bits unsigned. However, data going into the FIFO frame is 24 bits, after adding the saturation flag bit (from digital filter) as the Most Significant Bit (MSB).

12.5.1 Sensor Data Sampling into FIFO

There are two methods of sampling the data available in the FIFO: Polling Mode or Interrupt Mode.

In Interrupt Mode the host can wait till the interrupt line goes low in order to read data from the FIFO. The interrupt remains low till the FIFO is cleared from data.

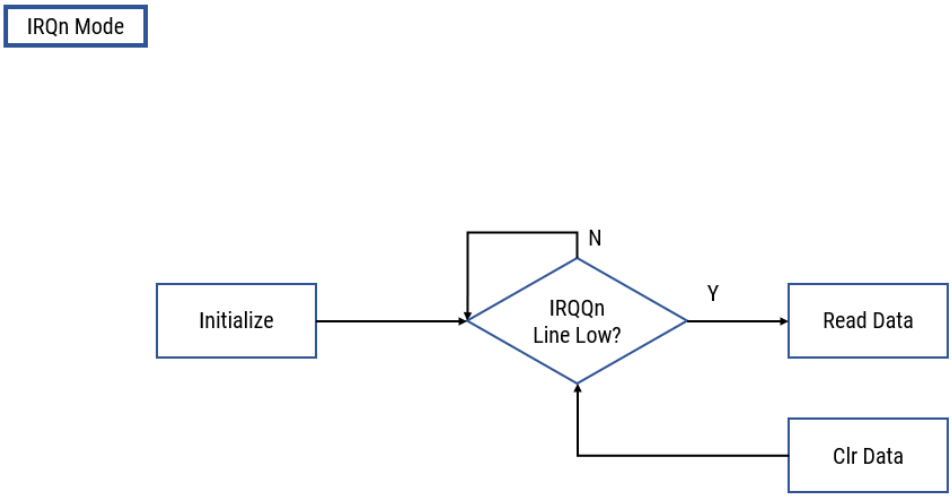

Figure 16 – Interrupt Readout Mode Flowchart

In Polling Mode the host has to read the FIFO status packet to determine if data is available in order to read it. The number of data packets available can also be determined from the status packet allowing multiple reads without having to keep reading the status packet.

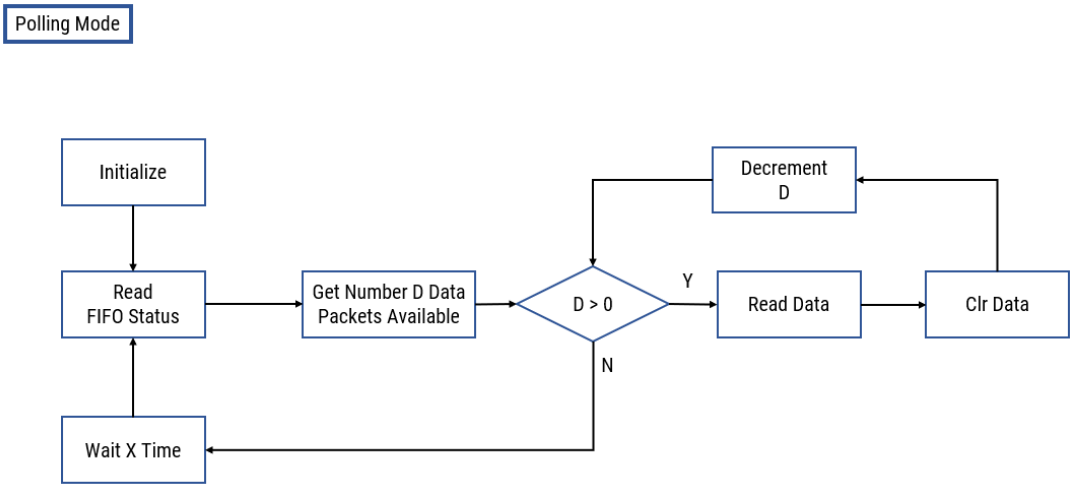

Figure 17 – Polling Readout Mode Flowchart

Additionally, when using Polling Mode, the interrupt pin can be disabled if not required.

12.5.2 Access to the FIFO

The internal clock is used to write data to the FIFO, while the I²C clock is used to read data from the FIFO.

For writing, using internal clock, a whole frame can be written without interruption. The writes will stop when the FIFO is full, even if more data frames are available from the ADCs. For reading, using I²C clock, which is controlled by an external host, it may read part of the frame and stop (in this case, this frame is unchanged, unless the host sends the FIFO_CLEAR command). The Read will be void if the FIFO is empty.[4]

12.5.3 Blocked and Incomplete Transfers

When the FIFO buffer is full, any new data will be lost. This happens when new sensor data frames arrive faster than Read + Clear_FIFO.

On the other hand, if a Read command is issued when there is no data in the FIFO buffer, the sensor as I²C slave will send a NAK (not acknowledged) to the host, after is receives the "SAD+R" byte.

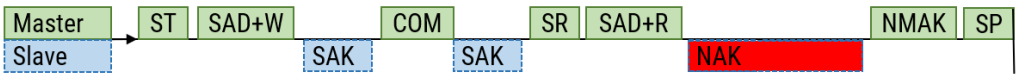

Figure 18 – Example of a Blocked I²C Transaction

There are ways for the I²C master to find out if the FIFO buffer is empty or full, as follows:

- **Observe the INT Interrupt Pin:** if it is high, then the buffer is empty.
- **Read the FIFO_Status:** if count = 0, then the buffer is empty; if count = 14, then the buffer stack is full.

[4] The FIFO_CLEAR command should be repeated after at least 1 data sample, if it is used consecutively.

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Furthermore, if the Read (from the FIFO buffer) is terminated earlier than expected (for example just reading 3 out of 5 channels, then stop), the FIFO pointer stays unchanged and so the user can read at the same frame again, if needed.

12.5.4 RAM Address Mapping

There are 14 frames in the FIFO and 17 bytes (5 channels of 3 bytes each + frame count of 2 bytes) in each frame. Hence, it requires 4 encoded bits for number of frame, FR[3:0], and 5 encoded bits for number of byte in each frame, CH[4:0]. However, there is 8 bits address for RAM, so need a mapping between them. It is proposed each data package (5 channels of 3 bytes each) is put in regular "0000----" to "1101----" of the RAM address and the frame count is put elsewhere, so that it is easy for mapping.

The code below shows the algorithm of mapping 9 bits Frame-Byte to 8 bits Ram address:

```
// convert from (4+5) Frame-Byte bits to 8 RAM address bits
If  (CH[4] == 0) then                          // first 15 bytes (5 channels of 3 bytes each)
        Adr     <= FR[3:0] & CH[3:0];
Else then                                      // last 2 bytes (frame count)
        Adr     <= "111" & CH[0] & FR[3:0];
End
```

The first 15 bytes (5 channels) of each frame, for 14 frames, are put in "regular" RAM address from 0 to 223, using all bits of FR[3:0], and 4 bits of CH[3:0]. The first byte of frame count, byte 16th, is put in address "111**0**----" and the second byte, byte 17th, is put in address "111**1**----".[5]

12.5.5 Response to I²C Command (CMD)

When the sensor is enabled, hence not in Power Down Mode, it always receives and responds to I²C commands – including simple set/reset instruction. For commands with data in/out, the device acts as in the following example:

- For Read Channel Control Packet, the sensor sends out 5 bytes of data (to the host) and expect an ACK (from the host) at the end of each byte.
- For Write Channel Control Packet, the sensor expects 5 bytes of data (from the host) and send out an ACK (to the host) at the end of each byte.

However, for the commands with only set/reset type of instruction (there are 7 such commands: Test, FIFO_Clear, FIFO_Reset, Go_To_Sleep, Wake_Up, Reset_Soft, Reset_Full), the device will treat them as Read commands, and will send back an Ok/Err byte, including the original command. For example with the command Wake_Up (code 0x24), the device will reply with a byte

- **If OK:** "10010001" - bit[6:2]: received code "0x24" in blue; bit[0]: OK bit in red
- **If Error:** "10010010" - bit[6:2]: received code "0x24" in blue; bit[1]: Error bit in red

In summary, the device treats all commands as Read or Write instructions, and never as "simple instruction" without any response. However, the host can stop a command at any time. So if the host does not need to read back the Ok/Err byte for those set/reset instruction, it can stop after sending the COM code.[6]

[5] The first 15 bytes is put in a "block" of 16 addresses. It uses address "0001" to "1111" and not use "0000".

[6] Apart from responding to an I²C command via I²C I/O, the device also generates an interrupt, which is the INT line being pulled low (active low) to indicate that
   a) *data is available while in Normal Operation Mode, or*
   b) *a wake up condition has been detected while in Sleep Mode.*

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12.6 Digital Interface

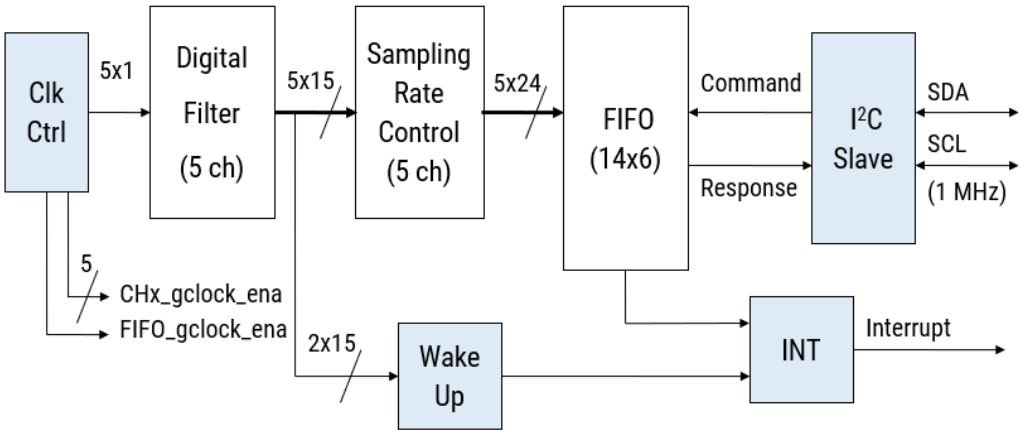

Figure 19 – Digital Interface Block Diagram

12.6.1 ADC and Digital Filter

The digital 1 bit stream from the Delta-Sigma modulator is filtered by a Sinc third order filter followed by a first order low pass filter. The filtered output is 15-bit wide. The sample clock frequency is 1 kHz (Normal Power Mode) or 166 Hz (Low Power Mode).

The output of the ADC is followed by a programmable first order low pass filter, the available frequencies are 180 Hz, 90 Hz, 45 Hz and 22.5 Hz in Normal Power Mode and 30 Hz, 15 Hz, 7.5 Hz and 3.75 Hz in Low Power Mode (see Table 8 for selection control).

The data (15 bits) at 1 ksps (1 kHz sample rate) or 166 sps (166 Hz sample rate) enters the Sampling Rate Control circuit and then is written to the FIFO.

12.6.2 Sampling Rate Control

The data from the ADC digital filter is accumulated into a 23-bit accumulator. However, it will send a total of 24 bits data to the FIFO, with the MSB being the saturation bit from the filter (indicating over-range condition). The number of accumulated base samples (at either 1 ksps or 166 sps) depends on the setting of the desired output frame rate. See section 13.3.6 on the AFEP register, Byte 0 for information on frame accumulation settings.

12.6.3 FIFO Stack

One data frame (package) consists of 5x3 bytes data from 5 channels, plus 2 bytes Frame-Count. In total, there will be 17 bytes in each data frame. The Frame Count is simply the rollover counter of the current data frame.

A FIFO stack consists of 14 data frames. It actually is a dual port RAM, with separated Read and Write pointers. When both pointers point at the same frame, an individual lock for Read and Write are needed. The size of the RAM will be 256 x 8 bits (but we will only use 14 x 17 = 238 address locations).

12.6.4 Sleep Mode and Wake Up Detection

When a GO_TO_SLEEP command is received:

- All channels are disabled except the active channel selected in the **Wake Up Packet**.
- The input to FIFO will stop accepting data and the FIFO will be flushed.
- The Wake Up circuit is active after 64 ADC samples (at 1 kHz, ~64 ms) in Normal Power Mode or 384 ADC samples (at 166 Hz, ~384 ms) in Low Power Mode and will generate an interrupt when the wake up conditions are met.

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When a WAKE_UP command is received:

- All channels are active as configured in **Channel Control Packet**.
- The FIFO will resume operation after 64 ADC samples in Normal Power Mode or 384 ADC samples in Low Power Mode. The delay is due to the time required for the analog channel to stabilize on power up.
- The interrupt will be cleared, and the sensor will resume in Normal Operation Mode.

The wake up detection works as per below description.

The data is coming from the selected channel in **Wake Up Packet**. There are two modes of operation:

- In one channel mode, the data of the selected channel (CHx) is used to determine the wake up event.
- In two channel mode, the data of the selected channel (CHx) subtract the Reference channel (DPx) will be used.

The result data output is compared to five digital programmable thresholds. When the data value (8 MSB) is between UHT and ULT (or LHT and LLT) continuously for a WL number of data sample, the wake up is detect and send an interrupt to the host.

Table 9 – Power Consumption in Sleep Mode (1.8 V, Room Temperature)

	Normal Power Mode (LP = 0)	Low Power Mode (LP = 1)
1 Channel Active	21 µA	3.5 µA
1 Channel + Reference Channel	35 µA	5 µA

12.7 Device Power Up and Reset

12.7.1 Common CS and V_{Supply}

For configurations where CS is shorted to V_{Supply} the device is initialised correctly by only applying power to these pins. Please note that in this case, and when multiple devices on one I^2C bus, an external mechanism needs to be implemented to power up devices in sequence in order to give each one a unique I^2C address.

12.7.2 CS Controlled by MCU

In order to re-enable the device after a power down using CS pin follow these steps:

1. Ensure the V_{Supply} pin is powered, while holding CS low (Power Down Mode).
2. Pull CS high for a minimum of 50 µs.
3. Pull CS low for 0.5 to 20 µs – recommended low pulse duration is 2 µs.
4. Set CS high – the sensor is now in Normal Operation Mode with all settings reset to their defaults.[7]

12.7.3 Reset Methods

There are three ways to reset the sensor:

- Pulling the CS pin low resets the entire device including analog and digital sections. All registers take their default values. It takes approximately 8 ms to complete this reset action.
- **I^2C Full Reset:** has the same effect as toggling the CS pin, however the device is not powered down and then up again. Therefore it takes only 100 µs to complete.
- **I^2C Soft Reset:** maintains register settings, while reinitialising every active channel and flushing the FIFO buffer.

[7] This sequence allows the sensor to stabilise reliably. The sensor may appear operational after setting the CS high for the first time (2). However there may be intermittent stability problems if this procedure is not followed.

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13 I²C INTERFACE

The IC acts as a slave I²C device compliant with the fast mode plus (1 MHz) I²C standard.

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy.

The next byte of data transmitted after the start condition contains the address of the slave in the first 7 MSBs and the eighth bit (LSB) tells whether the master is receiving data from the slave or transmitting data to the slave.

When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the device behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit command (COM) will be transmitted.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. The following table explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Transfer when master is issuing single command to slave:

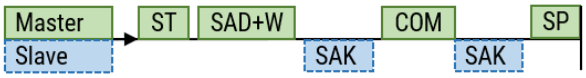

Figure 20 – I²C Transaction - Single Command

Transfer when master is writing one or more (N) bytes to slave:

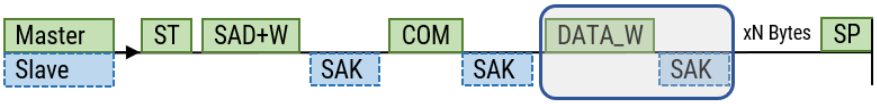

Figure 21 – I²C Transaction - Writing More than One Byte

Transfer when master is reading single byte from slave:

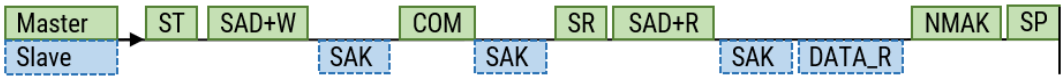

Figure 22 – I²C Transaction - Reading Single Byte

Transfer when master is reading multiple bytes from slave:

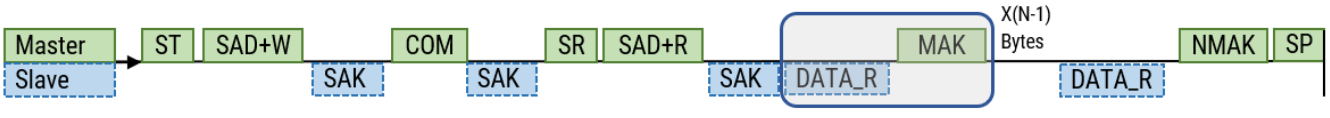

Figure 23 – I²C Transaction - Reading Multiple Bytes

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Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is given by the command. Data is transferred with the most significant bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (it is not able to receive because it is performing some real time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

Single command transfers can contain an optional Ok or Error reply, depending on if a Start Repeat or STOP condition has been issued.

13.1 I^2C Addressing

The default I^2C address is 1100101b and can be changed to any valid address by sending an I^2C command. The new address is valid for as long as the device is active and will reset to the default address once it is reset or powered off.

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13.2 List of I²C Commands

Table 10

Command[8]	COM Code	Data Type	Data Size (Bytes)	Data	Action
TEST	0x00	Command	1	OK/Err: 000000-01/10	Verify communication by reading the response packet
VERSION	0x02	Read	1	Version Packet	
FIFO_STATUS	0x04	Read	1	FIFO Status Packet	"WD, Err[1:0], FIFO_Cnt[3:0], iInt"
FIFO_READ_FULL	0x06	Read	17	14 Data Packets	Read full data packet (17 bytes) of all channels
FIFO_READ_ACTIVE	0x08	Read	up to 17	14 Data Packet Active	Read data packet (up to 17 bytes) for only active channel
FIFO_CLEAR	0x0A	Command	1	OK/Err: 001010-01/10	Clear the current packet (Read pointer moves on next)
FIFO_RESET	0x0C	Command	1	OK/Err: 001100-01/10	Clear the entire FIFO (Rd/Wr pointer reset with the empty)
CH_READ	0x0E	Read	5	Channel Control Packet	Configure each analog channel
CH_WRITE	0x10	Write	5	Channel Control Packet	
ANA _READ	0x12	Read	2	Analog Settings	
ANA _WRITE	0x14	Write	2	Analog Settings	
WAKE_READ	0x16	Read	6	Wake-Up Packet	Byte 6 is the channel active in Sleep Mode
WAKE_WRITE	0x18	Write	6	Wake-Up Packet	
ADDR_WRITE	0x1E	Write	1	I²C Address	7 MSB (default: 1100101b)
GO_TO_SLEEP	0x20	Command	1	OK/Err: 100000-01/10	Put the device in Sleep Mode
WAKE_UP	0x22	Command	1	OK/Err: 100010-01/10	Wake up and resume normal mode
RESET_SOFT	0x24	Command	1	OK/Err: 100100-01/10	See section 12.7
RESET_FULL	0x26	Command	1	OK/Err: 100110-01/10	See section 12.7

13.3 I²C Packets

13.3.1 Ok Packet (OKP - R)

Single byte echoing the command with 2 LSBs are "01", if an operation has been completed successfully.

OKP	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	Cmd 5	Cmd 4	Cmd 3	Cmd 2	Cmd 1	Cmd 0	0	1

Figure 24 – OK Packet (OKP) Format

[8] Commands are always 6-bit length or shorter. The command included in Ok and Error packets is bit shifted left by two bits with the 2 LSBs forming the Err/OK code.

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13.3.2 Error Packet (ERRP - R)

Single byte 0x02 returned if an operation has failed or error occurred.

ERRP	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	Cmd 5	Cmd 4	Cmd 3	Cmd 2	Cmd 1	Cmd 0	1	0

Figure 25 – Error Packet (ERRP) Format

13.3.3 FIFO Status Packet (FS - R)

Single byte with the status of the FIFO or Wake-Up algorithm.

FS	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	Wake Detected	Error 1	Error 0	FIFO Count 3	FIFO Count 2	FIFO Count 1	FIFO Count 0	Inversed INT Status

Figure 26 – FIFO Status Packet (FS) Format

- **Inversed Status (1bit [bit 0]):** in Normal Operation Mode, this bit is set (1) when the FIFO is not empty and reset (0) when the FIFO is empty. It is an inverse of Interrupt Pin Output (without masking).
- **FIFO Count (4 bits [bits 4:1]):** number of data packets available in the FIFO.
- **Error status (2 bits [bits 6:5]):**
  00 – no error.
  01 – write when FIFO is full (FIFO count = 14) or read when FIFO is empty (FIFO count = 0).
  10 – detect I^2C read FIFO early termination (read less bytes than expected).
  11 – detect I^2C read FIFO extra (read more bytes than expected).
  For example, command FIFO_Read_Full will expect to read 17 bytes from FIFO, but if the host stop reading before 17 bytes, then error = "10" and if the host try to read more than 17 bytes, then error = "11". In case of read more than 17 bytes, the Slave still responds with invalid data from byte 18 onward.[9]
- **Wake Detected (1bit [bit 7]):** 1 if in Sleep Mode and wake up event detected, 0 otherwise.

13.3.4 Channel Control Packet (CCP - R/W)

The Channel Control Packet contains 5 bytes, each of which corresponds to a single channel with its individual settings. Note that channel 0 is currently used for internal test purposes only.

CCP	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Byte 0 : Ch 0	C0_TC[1]	C0_TC[0]	C0_HP[1]	C0_HP[0]	C0_G[2]	C0_G[1]	C0_G[0]	C0_ST[0]	**0x00**
Byte 1 : Ch 1	C1_TC[1]	C1_TC[0]	C1_HP[1]	C1_HP[0]	C1_G[2]	C1_G[1]	C1_G[0]	C1_ST[0]	**0x00**
Byte 2 : Ch 2	C2_TC[1]	C2_TC[0]	C2_HP[1]	C2_HP[0]	C2_G[2]	C2_G[1]	C2_G[0]	C2_ST[0]	**0x00**
Byte 3 : Ch 3	C3_TC[1]	C3_TC[0]	C3_HP[1]	C3_HP[0]	C3_G[2]	C3_G[1]	C3_G[0]	C3_ST[0]	**0x00**
Byte 4 : Ch 4	C4_TC[1]	C4_TC[0]	C4_HP[1]	C4_HP[0]	C4_G[2]	C4_G[1]	C4_G[0]	C4_ST[0]	**0x00**

Figure 27 – Channel Control Packet (CCP) Format

[9] In case I^2C hung up, it can be detected internally, but cannot respond due to no activity of I^2C clock. However, it will reset itself at the new I^2C command.

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Table 11 – Channel Status Selection

Cx_ST[0]	Channel Status
0	Channel Disabled
1	Channel Enabled

Table 12 – Feedback Capacitor Selection

Cx_G[2:0]	Feedback Capacitance (fF)	Relative Gain
0	50	64x
1	100	32x
2	200	16x
3	400	8x
4	800	4x
5	1,600	2x
6 & 7	3,200	1x

Table 13 – High-Pass Signal Filter Frequency Selection[10]

Cx_HP[1:0]	High Pass Filter (Hz) Normal Power Mode	High Pass Filter (Hz) Low Power Mode
0	1	0.17
1	2	0.33
2	4	0.66
3	8	1.30

Table 14 – Front-End Transconductance Selection

Cx_TC[1:0]	Feedback Transconductance (Ω)
0	1.20 T
1	0.60 T
2	0.30 T
3	0.15 T

The channel settings are configured in Channel Control Packet. When this packet is modified (by the host) the current FIFO will be flushed automatically by the internal circuit. This will ensure the new active channel is applied to all new frames (going to the FIFO).

To flush the FIFO (same as I^2C command FIFO_RESET), the simplest way is to bring the Read pointer to where the Write pointer is and declare the FIFO empty, as described below:

- Once the Channel Control Packet is changed (by the I^2C command: CH_Write), the Read pointer is reset to the same position as the Write pointer.
- The flag (the MSB) of the Read pointer is also set to the same value as that of the Write pointer. This will imply an Empty in normal operation and hence prevent any Read.

[10] Must be enabled in Analog Front End Packet AFEP.

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13.3.5 Analog Front End Packet (AFEP - R/W)

The Analog Front End Packet contains the settings that control the common analog front end settings 2 bytes.

AFEP	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Byte 0	S7	S6	S5	S4	S3	S2	S1	S0	**0x00**
Byte 1	LP	HP	C_LP1	C_LP0	CLK_OUT	SYNC	0	INT	**0x09**

Figure 28 – Analog Front End Packet (AFEP) Format

- **S0-S7:** sampling rate (8 bit) – sampling rate = 1000/(N+1).
- **INT:** interrupt output – 1 enable, 0 disable (only apply at Normal Operation Mode and not in Sleep Mode).
- **Bit 1:** set to 0.
- **SYNC:** Sync & Clk pin option: 0 Master, 1 Slave.
- **CLK_OUT:** 1 enable internal clock output on Clk pin, 0 disable internal clock output on the Clk pin (only apply for Master. For Slave, this is ignored, because the Clk pin is used as input).
- **HP:** Enable high pass filter – 1 enable, 0 disable.
- **LP:** Enable Low Power Mode – 1 enable, 0 disable.

Table 15 – Low-Pass Signal Filter Frequency Selection

C_LP[1:0]	Low pass frequency (Hz) Normal Power Mode	Low Pass Frequency (Hz) Low Power Mode
00	180	30
01	90	15
10	45	7.5
11	22.5	3.75

13.3.6 I²C Address Packet (I2CADD W)

Single byte containing the 7 bit new I²C address.

I2CADD	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Byte 0	Addr6	Addr5	Addr4	Addr3	Addr2	Addr1	Addr0	XX	**0xCA**

Figure 29 – I²C Address Packet (I2CADD) Format

I²C address is shifted to MSB to make reading easier with read/write bit.

13.3.7 Wake Up Packet (WUP - R/W)

The Wake Up Packet contains the thresholds used in the wake up algorithm.

WUP	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Byte 0 : UHT Threshold	uht7	uht6	uht5	uht4	uht3	uht2	uht1	uht0	**0xFF**
Byte 1 : ULT Threshold	ult7	ult6	ult5	ult4	ult3	ult2	ult1	ult0	**0xFF**
Byte 2 : LHT Threshold	lht7	lht6	lht5	lht0	lht0	lht2	lht1	lht0	**0x00**
Byte 3 : LLT Threshold	llt7	llt6	llt5	llt4	llt3	llt2	llt1	llt0	**0x00**
Byte 4 : WT Threshold	wt7	wt6	wt5	wt4	wt3	wt2	wt1	wt0	**0x10**
Byte 5 : Ch Setting	XX	ST	dp2	dp1	dp0	ch2	ch1	ch0	**0x00**

Figure 30 – Wake Up Packet (WUP) Format

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- **Byte 0 to 3 (upper and lower thresholds):** these are the 8 MSB of channel ADC data (unsigned value).
- **Byte 4:** is the number of samples required to trigger the wake up algorithm.
  UHT and ULT to detect positive wake-up event (UHT > ULT)
  LHT and LLT to detect negative wake-up event (LHT > LLT)
  Number of sample where the signal is in between threshold (WT).
- **DP0-DP2:** the reference channel coding, and **CH0-CH2:** the selected channel coding.
  000 – select channel 0.
  001 – select channel 1.
  010 – select channel 2.
  011 – select channel 3.
  1xx – select channel 4.
- **ST:** Sleep Mode type.[11]
  0 – one channel sleep type, set by ch0-ch2.
  1 – two channel sleep type, set by both dp0-dp2 and ch0-ch2.

13.3.8 FIFO Data Packet Full (FIFO_DPF - R)

17 bytes containing the top frame available in the FIFO which has the channel data as well as a frame counter.[12]

FIFO_DPF	Data
Byte 0	Channel 0 bits 23:16
Byte 1	Channel 0 bits 15:8
Byte 2	Channel 0 bits 7:0
Byte 3	Channel 1 bits 23:16
Byte 4	Channel 1 bits 15:8
Byte 5	Channel 1 bits 7:0
Byte 6	Channel 2 bits 23:16
Byte 7	Channel 2 bits 15:8
Byte 8	Channel 2 bits 7:0
Byte 9	Channel 3 bits 23:16
Byte 10	Channel 3 bits 15:8
Byte 11	Channel 3 bits 7:0
Byte 12	Channel 4 bits 23:16
Byte 13	Channel 4 bits 15:8
Byte 14	Channel 4 bits 7:0
Byte 15	Frame count MSB
Byte 16	Frame count LSB

Figure 31 - FIFO Data Packet Full (FIFO_DPF) Format

- **Channel Data:** 24 bit unsigned value.
- **Frame Count:** 16 bit unsigned value.

[11] In two channel sleep type (ST =1), if the reference channel (DPx) is set the same as the selected channel (CHx), then the device will behave as one channel type. Otherwise, subtracting the same data will result zero and so can never be woke up.
The TEMP bit will be forced to 0 during the Sleep Mode.
[12] Bit 23 of each channel data indicates over range condition, when this bit is set, the frontend circuit output is out of range and it is resetting.

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13.3.9 FIFO Data Packet Active (FIFO_DPA - R)

Up to 17 bytes containing the top frame available in the FIFO which has only the active channel data as well as a frame counter (the example below shows channel 0 and 4 active).

FIFO_DPA	Data
Byte 0	Channel 0 bits 23:16
Byte 1	Channel 0 bits 15:8
Byte 2	Channel 0 bits 7:0
Byte 3	Channel 4 bits 23:16
Byte 4	Channel 4 bits 15:8
Byte 5	Channel 4 bits 7:0
Byte 6	Frame count MSB
Byte 7	Frame count LSB

Figure 32 – FIFO Data Packet Active (FIFO_DPA) Format

- **Channel Data:** 24 bits unsigned value**.**
- **Frame Count:** 16 bits unsigned value.

In this mode, the number of bytes sent will depend on number of active channels, for example, 2 channels (ch0 and ch4) active = 2 * (3 bytes) + (2 bytes frame counter) = 8 bytes.

14 HANDLING PRECAUTIONS

14.1 ESD

The performance of this device can be affected by ESD. Precautions should be used when handling and installing the sensor. Precision devices such as this sensor can be damaged or caused not to meet published specification due to ESD. Please note that there is limited ESD protection built-in as the device is optimised for low power consumption and low noise operation.

14.1.1 ESD Ratings

Human Body Model (HBM), per JS-001: 2000 V

Charged Device Model (CDM), per JESD22-C101: 500 V

14.2 Corrosive Substances and Cleaning Materials

The sensor must not be exposed to corrosive substances.

14.3 Moisture Sensitivity

The sensor is classed as Moisture Sensitivity Level 3 (MSL-3). The package should be handled according to IPC/JEDEC J-STD-20.

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15 PCB LAYOUT AND DEVICE MOUNTING

15.1 PCB Landing Pattern

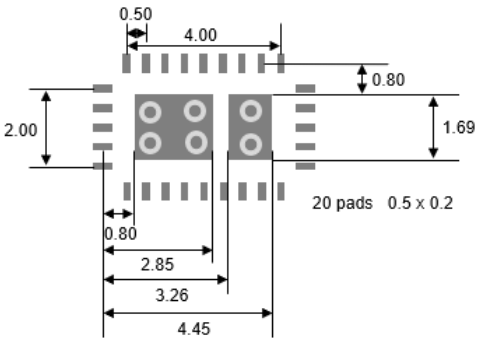

Figure 33 – Recommended PCB Landing Pattern

15.2 Soldering Process

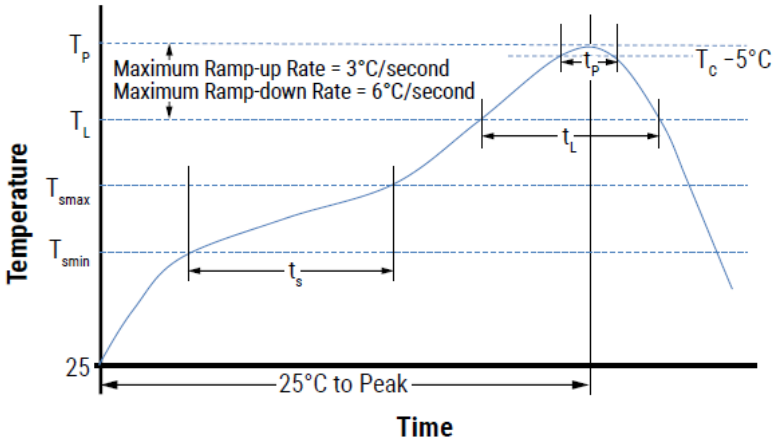

Figure 34 – Recommended Reflow Soldering Profile

Table 16 – Recommended Soldering Parameters

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Minimum (T_{smin}) Temperature Maximum (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60 – 120 seconds
Ramp-up Rate (T_L to T_P)	3 °C/second maximum
Liquidous Temperature (T_L)	217°C
Time Above Liquidous (t_L)	60 – 150 seconds
Peak Temperature (T_P)	260°C
Time within 5°C of Maximum Peak Temperature (T_p)[13]	30 seconds maximum
Ramp-Down Rate (T_P to T_L)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum

[13] Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and as a user maximum.

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16 TAPE AND REEL INFORMATION

16.1 Reel Dimensions

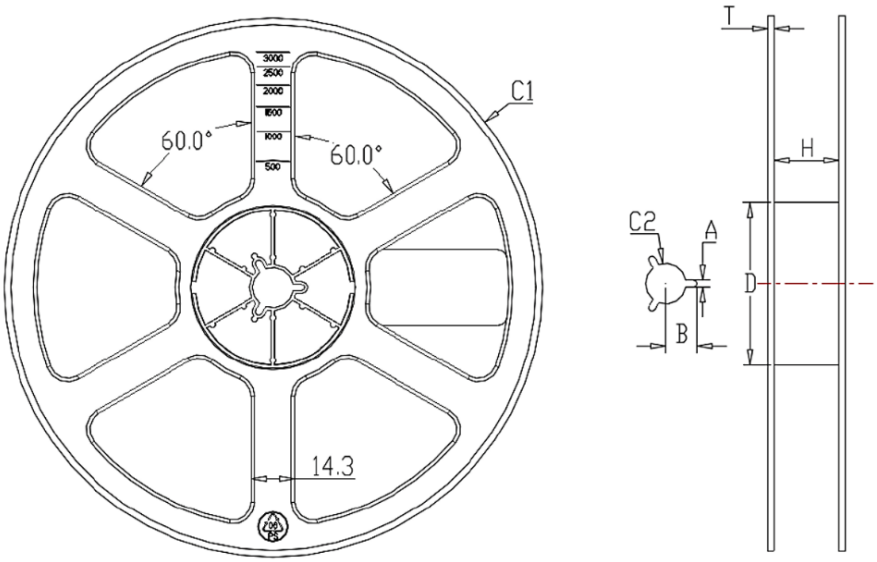

Figure 35 – Reel Dimensions Drawing

Table 17 – Reel Specification

	Tape Size	Dimensions (mm)							Units
		C1	C2	A	B	H	T	D	
Nominal	8 mm	Ø178	13.5	2.3	10.4	12.5	1.6	Ø54	800
Tolerance		±1.0	±0.2	±0.2	±0.2	±0.5	±0.2	±0.5	
Nominal	12 mm	Ø330	13.5	2.3	10.0	12.5	2.3	Ø100	4,000
Tolerance		±1.0	±0.2	±0.2	±0.2	±0.5	±0.2	±0.5	

16.2 Tape Leader and Trailer Dimensions

The tape trailer is 160 mm minimum in length and it consists of empty cavities with sealed cover tape. The tape leader is 400 mm minimum in length and it consists of empty cavities with sealed cover tape.

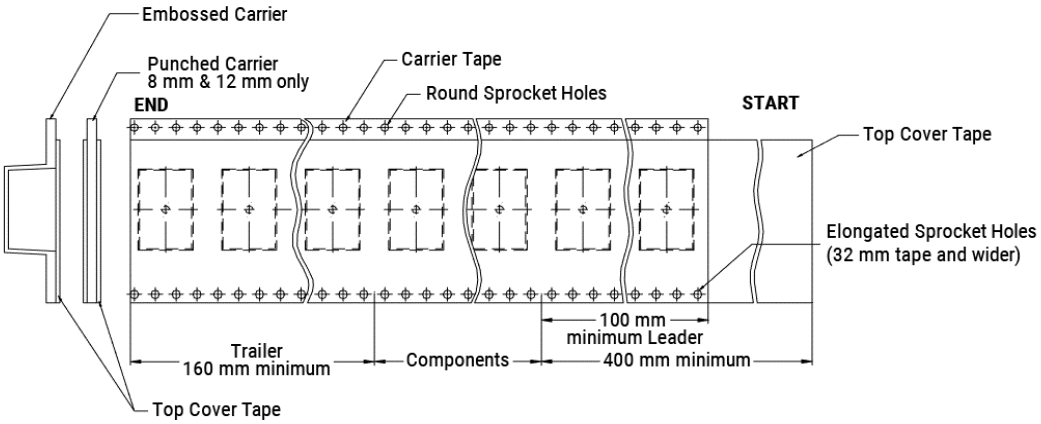

Figure 36 – Tape Leader and Trailer Drawing

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16.3 Tape Dimensions

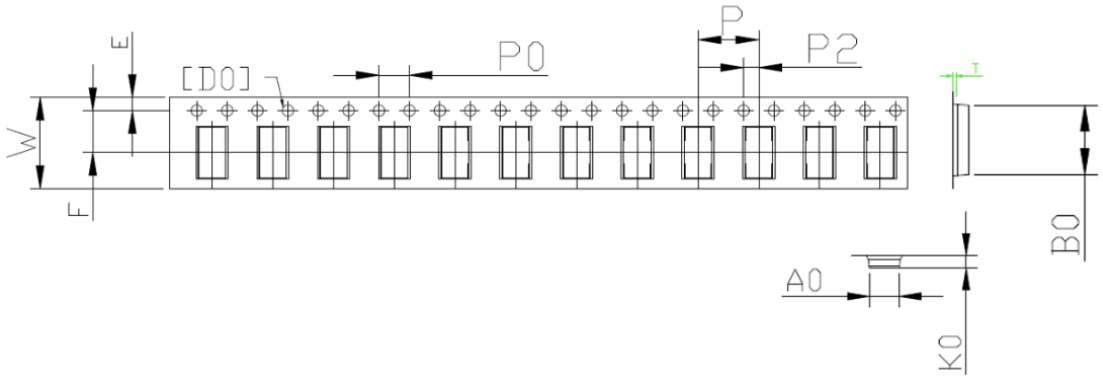

Figure 37 – Tape Dimensions Drawing

Table 18 – Taping Specification

	Dimensions (mm)										
	P0	P	T	P2	W	A0	B0	K0	E	F	D0
Minimum	3.90	7.90	0.25	1.90	11.70	3.90	5.85	1.65	1.65	5.40	1.50
Typical	4.00	8.00	0.30	2.00	12.00	4.00	5.95	1.75	1.75	5.50	1.50
Maximum	4.10	8.10	0.35	2.10	12.30	4.10	6.05	1.85	1.85	5.60	1.60

Cumulative tolerance of 10 pitches on tape ±0.2 mm.

Allowable camber to be 1 mm/100 mm (non-accumulative over 250 mm).

All dimensions based on EIA-481-2A standard.

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