Application Notes

MCU Sync Timing Control of Sensors ASICs

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DOCUMENT HISTORY

Version	Date	Change Ref.	Change Details
01	9 JUN 2020	N/A	First Release

1 INTRODUCTION

This application note covers the guidance for using an MCU to produce the signals for the sensor ASIC CLOCK and SYNC signals. This allows synchronisation of the sampling with an IR source being controlled by that same MCU.

2 HOW TO OPERATE SENSOR ASIC IN SLAVE MODE WITH EXTERNAL MCU AS TIMING MASTER

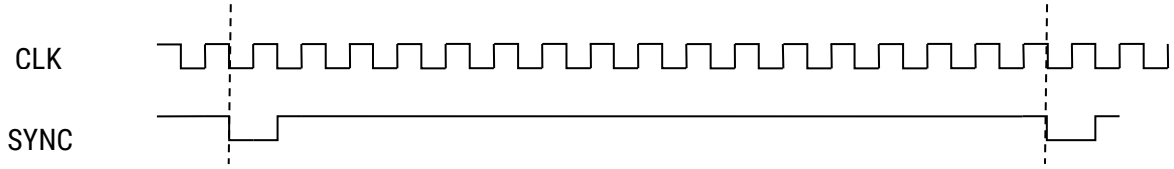

Figure 1 – Relationship between CLK and SYNC Pin

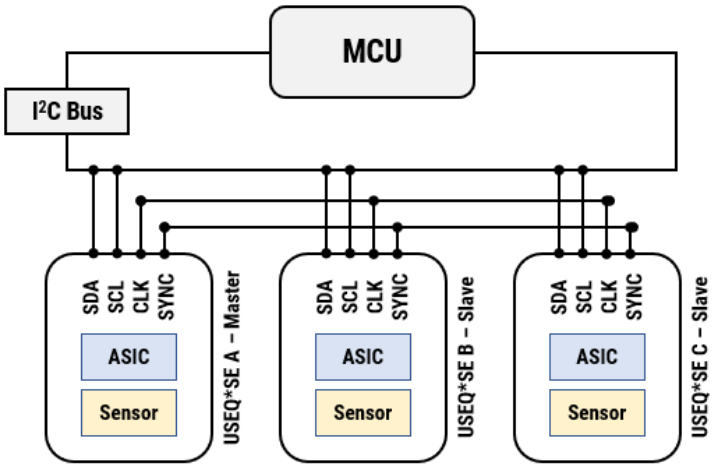

Figure 2 – Synchronisation Example: Three Devices with Synchronised Sampling

For a system with a master sensor ASIC and followed by multiple slave devices, the procedure is as follows:

- On the Master sensor ASIC, the Sync register bit should be set to 0, CLK_OUT should be set to 1.
- On the Slave sensor ASIC, the Sync register bit (bit 2 of Byte 1 in AFEP register) must be set to 1 and ignore the CLK_OUT register bit (bit 3 of Byte 1 in AFEP register).

- The Sync period is set by the byte 0 in the AFEP register of the Master ASIC. Note: byte 0 in the AFEP register of the Slave ASIC is also ignored.
- Connect the CLK and Sync signal from the Master to all the Slaves.

To simulate the behavior of the Master sensor ASIC by a microcontroller, these conditions should be met:

- The Clock signal should be ~32 kHz +/- 2.5% with a duty cycle between 45-55%.
- The Sync signal (at SYNC Pin) will be active (low) for 1 clock period, starting at (or after) the falling clock edge (but must be high before the next rising clock edge).
- The Sync period (simulate the behavior as per byte 0 setting in the AFE register) should be: (value+1)*32 clock cycle. If a value 10 is desired, then the Sync signal will be 351 clock periods high and 1 clock period low (Sync period is: (10+1)*32 = 352).
- The data will be ready after the rising edge of the Sync signal.