

# Improved Ripple Current Capability with Facedown Terminations

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## Abstract

The facedown termination design was originally devised to improve volumetric efficiency and lower ESL for tantalum surface mount capacitors. These goals have been met with this design change. It has also been found that this termination design improves power capability in a manner that is similar to power semiconductors that have been designed with this termination concept. The thermal resistance is dramatically decreased which creates a much more efficient transfer of heat out of this package. The power capability of these capacitors is determined by an allowable temperature rise and the ripple current is derived from this power and the ESR of the device at that temperature. We will demonstrate the changes in ESL, the wider impedance response allowing a reduced ceramic count, and the higher ripple capability created by the switch to this package.

## Facedown Termination

Since the tantalum-polymer's inception, it has been packaged as the previous tantalum-MnO<sub>2</sub> surface mount capacitors that had preceded it for the past 20 years<sup>[1]</sup>. A cross-sectional drawing in Figure 1 shows that entire device is encased in a plastic mold compound with electrical connection created by leadframe elements extending from encased connections to the outside, opposing, vertical faces of the plastic encapsulant. The cathode portion of the leadframe is normally attached to the upper face of the pellet using a conductive epoxy. The anode portion of the leadframe is welded to the tantalum riser wire. The leadframes are bent down against the vertical faces and folded under and along the bottom face to afford electrical contact to the solder pads on the circuit board.

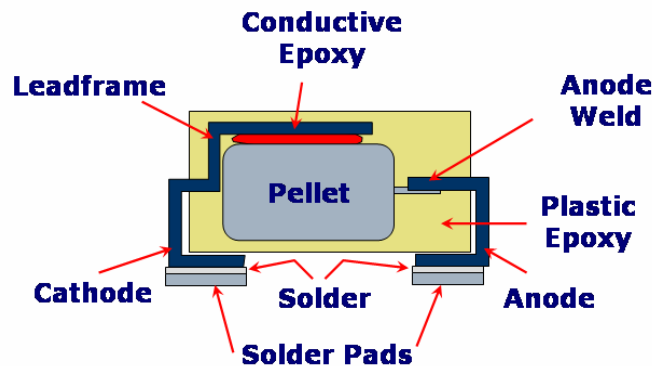


Figure 1. Standard surface-mount tantalum capacitor cutaway drawing.

The capacitive portion of the device is encased within the pellet structure. Except for the leadframe sections that extend out from the vertical faces of the plastic, the initial assembly of the pellet, epoxy, and leadframe must be isolated from the outside world by a wall of the plastic. This insulation requirement decreases the available volume of the plastic case to allow for a safe, consistent wall of plastic around all 8 faces for the initial assembly.

The pellet structure within this assembly is the centralized location of the capacitance created in this device. As shown in Figure 1, the pellet comprises a small portion of the devices total area of the diagram, thus a small portion of the case volume.

In Figure 2, the cross-sectional drawing of the facedown device highlights the tremendous differences. The only leadframe visible with this device is at the bottom face of the assembly (since these appear only in one plane or face of the device it is acceptable to refer to these contacts as plates). The pellet is attached to the bottom plate with a film of conductive epoxy. This connection is important, as we will show later on that this hard, full-face connection affords very little restriction in heat transfer from the pellet to the PCB. The riser wire is again welded, but to a vertical post created by splitting a tab structure from the anode leadframe. There remains a required plastic wall at the top, side, and end faces of the assembly, but because the bottom face is the contact face, there is no required insulative plastic along the bottom face.

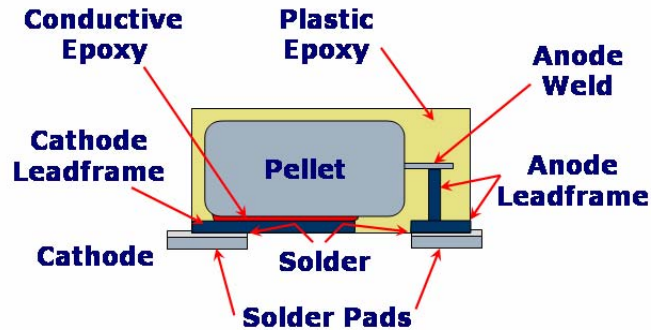


Figure 2. Cutaway view of facedown surface mount tantalum capacitor.

The improvement in volumetric efficiency is detailed in Figure 3. For the smaller cases detailed, the increase in volumetric efficiency is substantial. The first device created was to fulfill a specific demand, and was a “T” case (low profile “B” or EIA-3528 case) of dimensions 3.5 mm length, 2.8 mm width, and 1.2 mm height (Figure 4). The cathode contact is slightly larger than the anode and when soldered to the prescribed pads, the inside edges (vertical edges in drawing) of these pads help to align the device end-to-end, while the outside edges (horizontal edges in drawing) align the device side-to-side. The final alignment should allow edges exposed to afford solder pad contact for repair or replacement. If the solder pads were reduced to “fit” this device and allow a uniform exposed pad length, the area per chip could be reduced by 20% over the conventional pad arrangement.

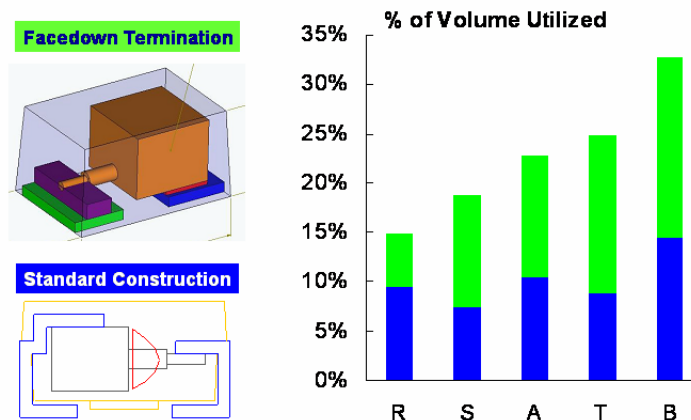


Figure 3. Volumetric efficiency improvement with facedown versus standard leadframe designs.

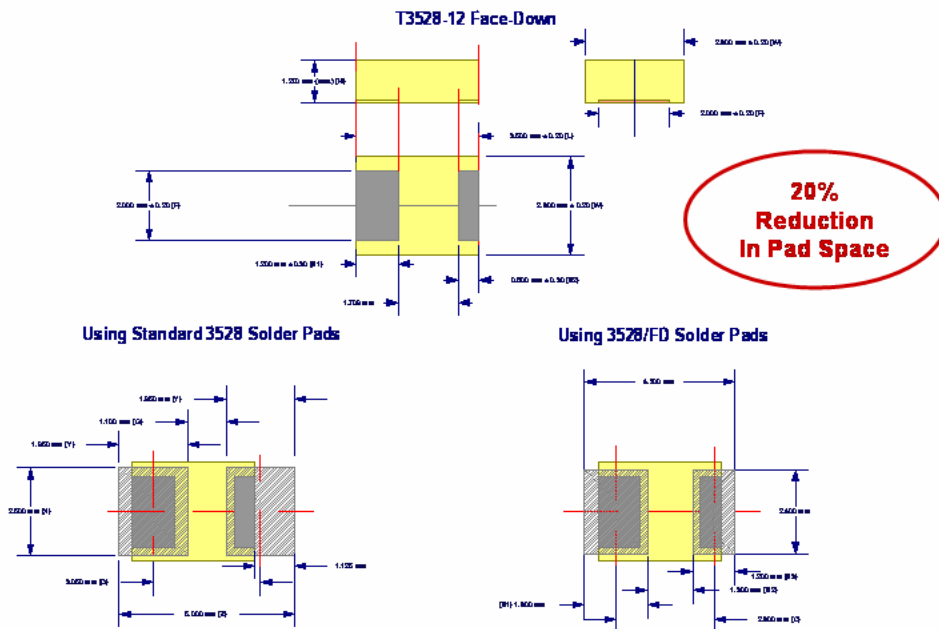


Figure 4. Solder pad dimensions and coverage for EIA 3528-12 case size.

The targeted application of this device was a hand held MP3 player, and the higher capacitance and lower profile of this device were the circuit's requirements.

### Lowered ESL

With our initial electrical testing, we soon realized that this device had a large drop in ESL from the standard 3528 case sized device. The reduction was by over 50%, (from 2.1 nH down to 0.9 nH) but with the capacitance and ESR attainable in this case size, the shift in ESL was not a significant factor in the impedance as the impedance minimum is controlled by the ESR. The reason for the ESL reduction is that the facedown design created a smaller current loop through the part as compared to the standard design (Figure 5) [2].

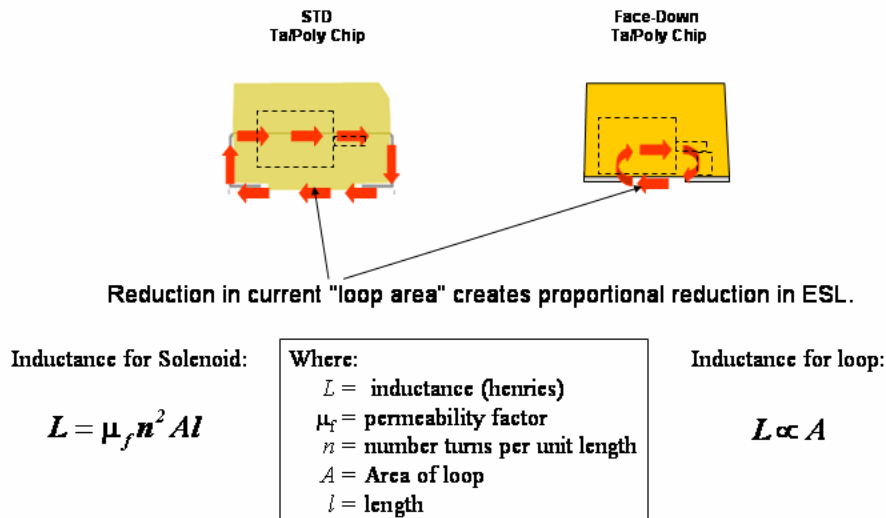
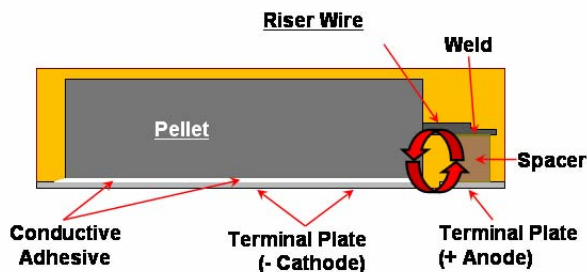


Figure 5. Standard versus facedown leadframe current loops in surface mount capacitors.

In order to see a significant performance advantage in lower ESL we needed to build a device with lower ESR, so that this reduction is significant. This required achieving an ESR below 10 milliohms, and the only devices we were building with this capability were the larger case sizes, or variations of the EIA-7343 size. ("D" case is one of these devices.) We

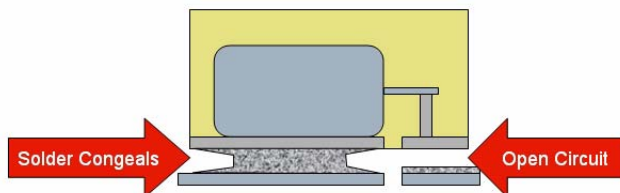
were initially stopped in the development of this device because Sanyo<sup>[2]</sup> released a “TPL” series capacitor in this case size with the specific advantage of lowered ESL. In addition, Sanyo built their device in such a manner that three plates were now visible on the bottom face of the device, and they secured patent protection on any such capacitor with three or more termination faces on the bottom surface.



**Figure 6. Lower ESL with minimized loop in EIA-7343 case size.**

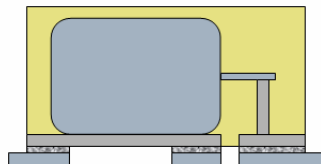
Our intention was not to build a three-terminal device, but to build a two-terminal device (Figure 6) because the capacitor has only a cathode and anode connection. We proceeded with our design, but we needed to make this device as compatible with the existing “TPL” recommended solder pads as possible (“he who is first, make the rules”). The separation between the anode and cathode plate was made compatible at 1.1 mm as this fulfilled our desire to keep this spacing as small as possible. We used a tantalum-polymer structure to allow the ESR to be as low as possible<sup>[3]</sup>. Initial designs used a spacer to bring the anode leadframe contact in line with the protruding riser wire. (This was replaced with a tab created from the anode plate to present an offset, vertical element to be bonded to.) Our testing revealed the ESL to be between 500 and 600 pH – thereby achieving a successful decrease from the 2,100 pH contained within the standard design.

We did not split the cathode plate and presented the device with two terminals, but of vastly different areas. The solder pads normally represent a similar shape to that of the metal faces in contact with it. If we were to create two solder pads with vastly different areas, there was concern that the solder on the larger pad would contract during the reflow process, thus lifting the chip and breaking the solder connection for the smaller anode pad (Figure 7).



**Figure 7. Using solder pads that mirror terminals could create open circuit conditions during solder.**

Because the Sanyo device recommended three-pad solder attach, we built the two-terminal device to fit on these three pads, and breaking the cathode contact to be soldered at two distinct and smaller pad locations, the problem with solder lift was eliminated (Figure 8).

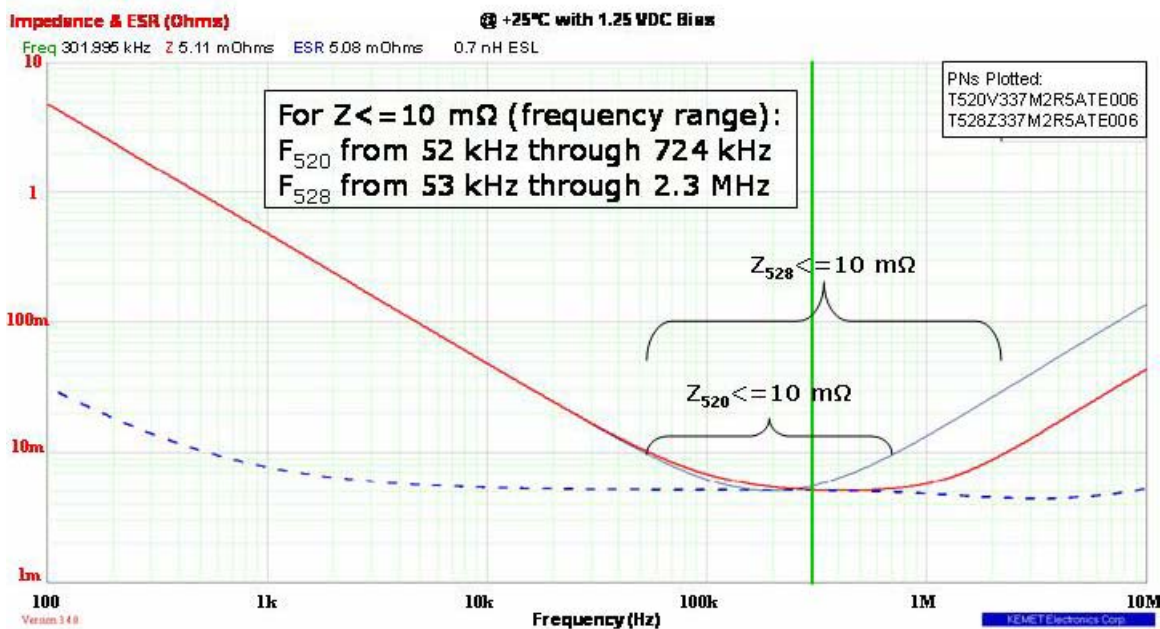


Requires 3 Solder Pads to prevent large pad from lifting.

**Figure 8. Soldering two-terminal device to three-pad layout eliminates solder lift.**

## Expanded Ripple Current Capability

With the facedown designs, we have now impacted the volumetric efficiency, and lowered the ESL<sup>[4]</sup>. The third highlight with this product is the expanded ripple capability. The Impedance and ESR of these devices versus frequency is shown in Figure 9. Both of these devices are the same physical size, same capacitance, voltage rating, and ESR. Looking at an arbitrary impedance level of 10 milliohms, the T520 (standard leadframe design) stays below that impedance level from 52 kHz through 724 kHz. This is the typical “bulk” capacitance decoupling range in the microprocessor decoupling schemes<sup>[5]</sup>. For the facedown device (T528), the range starts at 53 kHz but goes to 2.3 MHz before the impedance rises above 10 milliohms.



**Figure 9. Impedance and ESR vs. Frequency for T520 vs. T528 – equal parts.**

The difference in impedance levels are the result of the differences in the ESL for these two devices. The distinction is in the higher frequencies, above resonance, where the impedance is dominated by the inductive properties of the device. In Figure 10, the capacitance is plotted against frequency. The point of resonance is just above the point where the capacitance appears to drop to zero. For the T520 (standard leadframe) this point is at 199 kHz, while for the facedown (T528) this point is at 380 kHz. This near doubling of the resonant point is accomplished by nearly a 4 to 1 drop in ESL (2.19 nH for standard design versus 689 pH for facedown, at 10 MHz). Again, this difference is attributable to the change in ESL.

From Figure 10, the capacitance decay versus frequency is not affected by the change in ESL. This effect is strictly factored by the capacitance and ESR elements of the RC-Ladder, and since these elements within the pellet structures are identical, the response is identical. Small resistive differences created by the leadframe element of the standard design have no significant impact on the capacitance roll-off. At 301 kHz, the capacitance for the standard design is 270 uF, and for the facedown device is 272 uF.

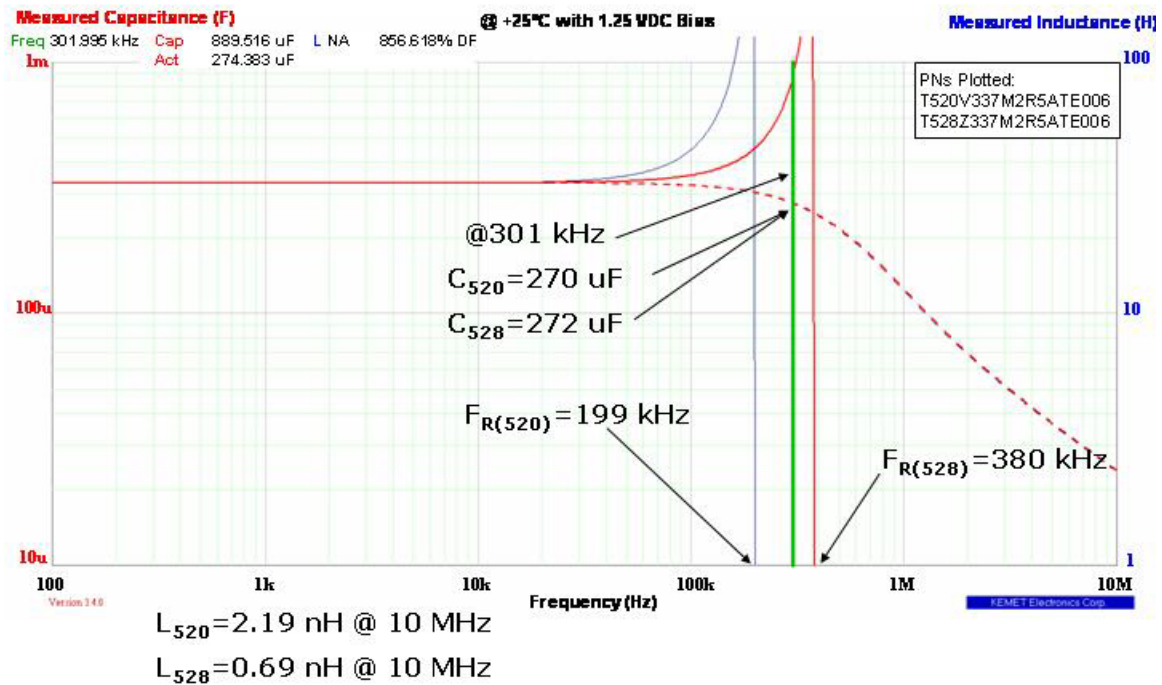


Figure 10. Capacitance versus frequency for the standard design (T520) and the facedown design (T528).

Now, looking at ripple current versus frequency (Figure 11) the additional benefits of the facedown design are highlighted. The ripple current is the result of the power dissipation capability of the device and the ESR. Since the ESRs are nearly identical, it is the power dissipation that changes dramatically in the facedown device.

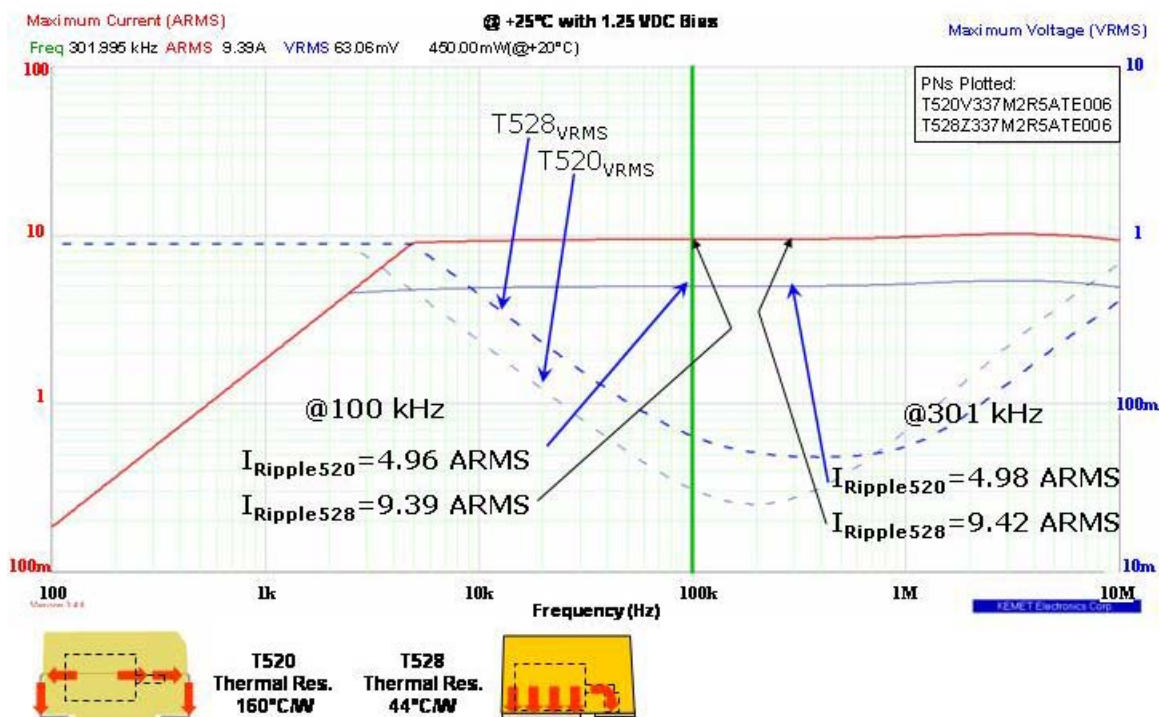


Figure 11. Ripple current versus frequency for the standard design versus the facedown design.

In Figure 11, the ripple capability of the facedown design is nearly twice that of the standard design. In the lower left of Figure 11, there is a small diagram that details the thermal transfer from the device to the PCB. Almost all of the heat dissipated by these devices is conducted heat – the plastic restricts radiation cooling because it has high thermal resistance.

Looking at the path in the standard device, the source of the heat is mostly in the pellet structure. Heat must pass from the pellet, into the leadframes extending out of the anode and cathode sides, then down to the PCB, then into the solder pads and eventually to the power and ground planes in the PCB.

For the facedown design, the transfer from the pellet is mostly through the full-face contact of one side of the pellet, through the thin film of conductive epoxy, into the broad surface of the leadframe then the solder to the PCB ground plane. The impact on power dissipation is tremendous. The thermal resistance for the standard device (T520) is around 160°C/Watt, and at 44°C/Watt for the facedown design (T528). At 100 kHz, the ripple capability for the facedown is 9.39 ARMS, while it is 4.96 ARMS for the standard design. This difference holds this difference from 50 kHz, up past 10 MHz.

### **Ideal Controlled ESR – Lossy Capacitor**

In discussions of increasing the ESR of ceramic capacitor, the ideal response is sometimes referred to as a lossy capacitor. The extremely low ESR of the MLCC creates very low impedance levels well below the targeted load-line impedance for many microprocessors. Adding ESR to these devices is not easily achieved, whereas changing the impedance levels for the lossy tantalum-polymer capacitors has already been demonstrated with the T528 facedown device. Our estimates are that we will be able to lower the ESL below 100 pH, and this will extend the low impedance trough of these capacitors well beyond 20 MHz – the upper levels required for board level decoupling.

### **Conclusions**

Regardless of the changes created in new designs, unless it offers a cost or space savings reward it will not become a mainstream product. The facedown device offers multiple opportunities in both venues. As it extends the boundaries of the lower impedance response, it could eliminate some of the hard to get and more expensive, high-CV MLCCs.

There are applications where multiple, standard devices are placed not to attain a specific impedance or ESR effect, but because of the total ripple experience of the PS must be shared across multiple devices to keep them within a safe operational range. The high ripple capability of the facedown, T528 device can certainly reduce piece counts, and board space in these instances.

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