

# ROCK SOLID AND UNDER 10 m $\Omega$ NEW HEAT AND MOISTURE-STABLE, LOW-ESR TANTALUM CHIP CAPACITORS

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## ABSTRACT

A tantalum chip capacitor having equivalent series resistance (ESR) less than 18 m $\Omega$  was described last year at the 19th Capacitor and Resistor Technology Symposium. The technological forces that drove the development of this device were detailed in that paper and a prediction was made that ESR requirements would fall by half every 1 to 1.5 years if the trends of the last 5 years were to continue. Also it was predicted that the ESR of individual capacitors would have to fall at least this quickly if a manufacturer wished to remain competitive. The demand for capacitors having ever-lower ESR continues unabated. In this paper is described the next step in the evolution of ultra-low ESR surface-mount tantalum chip capacitors -- devices boasting ESR lower than 10 m $\Omega$ .

Not only must ESR be ever-lower with each new generation of low-ESR capacitors, but also it is becoming ever more crucial that the ESR of these capacitors be stable during the solder-reflow mounting process and over their operational life. Environmental threats include exposure to reflow temperatures between 200C and 250C, moisture, thermal shock, and long-term exposure to temperatures well above 100C. The latest-generation, low-ESR tantalum chip capacitors described here take advantage of an optimal combination of materials and methods to produce devices that not only have exceptionally low ESR, but also have ESR stability that is nothing short of phenomenal in the face of severe environmental stress. The general principles and strategies used to develop these new capacitors are described and data are presented to document the stability of the resulting devices when they are exposed to multiple IR reflows, moisture, thermal shock, and long-term life test at elevated temperatures.

## INTRODUCTION

In 1998, Reed, Marshall, and Prymak<sup>1</sup> introduced a low-ESR tantalum chip capacitor whose guaranteed 30 m $\Omega$  ESR resulted from a novel, multiple-anode configuration. This device represented a 2-3 times improvement (reduction) in ESR over conventional single-anode tantalum chip capacitors of similar capacitance and case size. A compelling case was made that such reductions in ESR were needed, if for no other reason, just to reduce to manageable numbers the sheer quantity of capacitors required to achieve adequate power supply filtering for modern microprocessors.

The general operation of such power supplies was described and it was demonstrated that the number of capacitors required to achieve acceptable power supply performance is directly related to the ESR of these capacitors. It was also pointed out that ESR reduction results in higher efficiency, lower temperature rise, and improved device reliability.<sup>2</sup> The ESR-reducing nature of the multiple-anode design was explained and reliability data were presented to justify the claim that ESR reduction need not be purchased at the cost of reduced reliability.

In 1999, Reed and Marshall<sup>3</sup> introduced an 18 m $\Omega$ , multiple-anode tantalum chip capacitor. This device represented the next evolutionary step in ultra-low ESR tantalum chip capacitors. The authors prefaced their discussion of the development of this device with a historical review of the power requirements of a family of popular microprocessors. It was shown that easily-quantified trends of increasing processor current and decreasing processor voltage with time demand dramatic, but predictable, reductions in capacitor ESR to satisfy power-supply filtering requirements. Specifically, ESR must fall by half every 1.0 to 1.5 years to satisfy microprocessor power requirement trends.

The methodology of the design team was described. The team's approach was to create an electrical model of the multiple-anode design that accurately accounted for the ESR contribution of each of the readily identified sources of resistance in the finished device. This approach allowed the team to concentrate their ESR-reduction efforts on parts of the design that would yield the greatest overall improvement in finished-device ESR. The electrical performance of these capacitors was thoroughly explored and reliability data were presented to, again, demonstrate that very-low ESR and high reliability are not mutually exclusive.

Building on the foundation outlined above, ESR has been cut almost in half once again. Not only has a tantalum chip capacitor been fabricated whose initial ESR is guaranteed not to exceed 10 mΩ, but also remarkable improvements of ESR stability, in the face of severe environmental stress, have been demonstrated. Indeed, the capacitors described here are suitable for use in environments previously thought to be far too harsh for surface-mount tantalum chip capacitors.

Three key materials within these capacitors that directly impact low-ESR performance and ESR stability in the face of severe environmental stress are discussed: the carbon layer, the silver paint layer, and the terminal (leadframe) metal. Superior materials and methods have been identified that lead to exceptionally-low initial device ESR. A somewhat unexpected fringe benefit is that the combined use of these superior materials also produces unexpected ESR stability upon exposure to severe environmental stress.

Some considerations involved in the selection of a superior candidate from each of the three categories of key materials are discussed. Median ESR data culled from a designed experiment are presented that highlight the ESR-reducing benefits of the superior materials and, furthermore, demonstrate synergies among the superior materials that become evident only after severe environmental exposure. Finally, parametric data, including high-temperature life test data, from this designed experiment are presented to further emphasize that radical reduction of ESR and phenomenal improvements in ESR stability do not have to negatively impact overall device quality.

### **KEY MATERIALS USED IN ULTRA-LOW ESR CAPACITORS**

The majority of surface mount tantalum chip capacitors are manufactured in roughly the following manner: (1)

tantalum powder is compacted into a slug and then sintered to achieve a porous body of around 50% theoretical density. A tantalum wire is either pressed into the slug prior to sintering or is butt-welded to the slug after some degree of sintering. The tantalum wire serves as the positive electrical connection to the porous tantalum slug while the substantial exposed surface area of the porous slug serves as the positive plate of the capacitor. (2) An oxide film is electrolytically formed on the exposed tantalum surface of the slug. This oxide film is the dielectric of the capacitor. (3) The oxide-coated slug is repeatedly dipped in manganous nitrate and heated to convert the manganous nitrate to manganese dioxide, a semiconducting solid which costs the oxide film and serves as the negative plate of the capacitor. (4) The manganese dioxide coated slug is then dipped into a suspension of finely-ground carbon particles which is dried/Cured. The resulting carbon layer serves as a chemical buffer between the manganese dioxide and the following layer. (5) The carbon-coated slug is then dipped into silver paint and the resulting highly-conductive layer is dried/Cured. The silver paint serves as the negative electrical connection to the now fully-functional capacitor element. (6) The capacitor element is then electrically bonded to tabs on a punched metal leadframe assembly; the positive connection is made by welding and the negative connection is made with conductive adhesive. (7) A plastic case is molded around each slug, each individual molded capacitor is cut from the supportive leadframe assembly, and the portions of the metal terminal tabs which remain protruding from the molded case are folded under the case to act as the external, solderable terminals of the finished surface mount chip capacitor. Of course, considerable variation occurs from manufacturer to manufacturer, and, recently, multiple-element devices have been manufactured as is mentioned in the introduction.

Of the various materials mentioned above, three materials are found to be key to the superior performance of the capacitors described here: the carbon, the silver paint, and the metallic leadframe. One does not want to downplay the importance of optimizing the various other materials, but in this case, the lion's share of improvements in the other materials had already been made on previous generations of low-ESR devices.

As mentioned above, the carbon layer serves as a chemical buffer between the manganese dioxide and the silver paint. Absence of the carbon layer significantly raises ESR and many believe that the cause is oxidation of the silver in the silver paint by the oxygen-rich

manganese dioxide. Also, the ESR of the capacitor element will increase if the carbon layer is too thick, if its bulk resistivity is excessively high, or if gaps exist between the carbon and the layers it separates. A superior carbon suspension consists of finely-ground graphite particles which are suspended in a low-viscosity medium and mixed with a binder that decomposes to conductive species at elevated temperatures. A superior carbon coat is one that is just thick enough to effectively separate the manganese dioxide from the silver paint while conforming intimately to their surfaces without gaps or separations.

The purpose of the silver paint is to provide an essentially equipotential surface to collect the displacement currents that charge and discharge the capacitor during operation. It also serves as a surface that can be easily and effectively bonded with conductive adhesive to the negative portion of the leadframe assembly. If the bulk resistivity of the dried/cured silver paint is excessive, the ESR of the finished device rises because voltage drops exist along the surface of the paint between more distant portions of the capacitor element and the point of bonding of the silver paint to the leadframe (terminal) metal. To some degree this problem can be offset by making the paint layer thicker, but excessively thick layers can also add resistance and always consume volume within the device that could otherwise be used for additional capacitance or increased rated voltage. A superior silver paint contains a high percentage of silver flake, contains a thermally-stable binder, and has very low mobile ionic content after curing. A superior silver paint coat is thin, coats almost all of the capacitor element's surface, has very high electrical conductivity, and is mechanically stable when exposed to severe environmental stresses (humidity and/or temperatures above 120C).

The leadframe metal initially serves to aid the process of mass-production, but ultimately provides the metallic terminals that connect the capacitor element(s) to an external circuit. The leadframe contributes to the ESR of the finished device in several ways. Simple metallic resistance adds directly to the capacitor's ESR. More subtle is the resistance that occurs at the interface between the conductive adhesive and the leadframe metal where the silver paint coat of each capacitor element is bonded to the leadframe. This resistance also contributes directly to the capacitor's ESR. Any oxidation, corrosion, or growth of intermetallic species at this interface can severely increase ESR. Frequently, these ESR increases appear only after environmental exposure. A superior metallic leadframe has high

electrical conductivity, has a non-melting (at reflow temperatures) protective plating on the surface that is bonded to the silver paint of the capacitor element(s), has a suitable protective coating on appropriate surfaces external to the molded case to enhance either solderability or bonding via conductive adhesives, and has a suitable balance between ductility and mechanical strength.

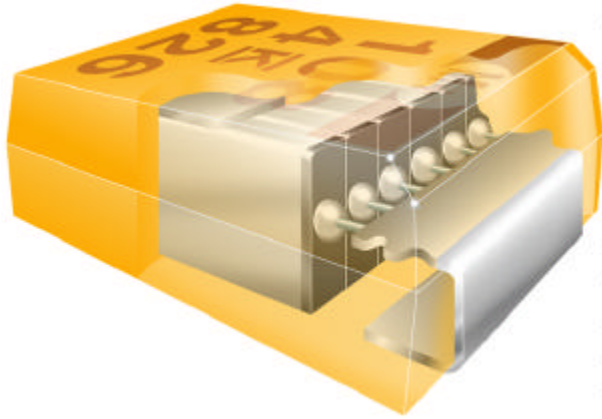
## **EXPERIMENTAL TRIALS**

A variety of candidate materials within each of the three key types of materials mentioned above were evaluated. Ultimately, one superior material was identified in each category and methods were developed to optimize its use in the manufacture of ultra-low ESR capacitors. Designed experiments were employed during these evaluations. A final, experimental trial was performed to confirm the efficacy of each superior material and to explore any interactions among the various superior materials. The results of this final designed experiment are discussed here.

The primary device characteristic of interest during these trials was 100 kHz ESR. Capacitance, dissipation factor, and D.C. leakage current data were also collected and will be discussed subsequently, but for brevity will not be discussed in this or the next section. Not only were ESR data collected "as manufactured," but also ESR data were collected after the capacitors were exposed to a series of environmental stresses. The environmental stresses were (1) three IR reflows using a standard IR reflow thermal profile, (2) 134 hours of unbiased HAST (highly accelerated stress testing) exposure at 121C and 85% RH, (3) 500 cycles of thermal shock between extreme temperatures of -55C and 125C, (4) 1000 hours of 150C life test at 0.5 times rated voltage, and (5) 1000 hours of 175C life test at 0.5 times rated voltage. These environmental stresses were cumulatively applied to the same set of test capacitors.

The devices described here are multiple-element tantalum chip capacitors that contain 6 elements. They are designed to have 1000 uF of capacitance and are rated at 4 Vdc. A cutaway view of a typical device appears in Figure 1.

Eight groups of capacitors were manufactured, representing a full-factorial experimental design in three variables. Two kinds of carbon, two silver paints, and two leadframe materials (including selectively applied protective platings) were employed, resulting in the eight experimental combinations. The two kinds of



**Figure 1. Physical Construction Details of a 1000 uF, 4V Multiple-Anode Tantalum Chip Capacitor.**

each key material are identified as either conventional or superior in the subsequent tables and discussion to avoid identifying specific manufacturer's products. More specific identification of these superior materials and details of their optimal application will appear in patents that have been applied for and will issue in the future.

The median 100 kHz ESR values for each of the experimental groups appear in Table 1. ESR data were measured for the devices as manufactured and after cumulative exposure to each of the five environmental stresses. The median ESR value is the ESR that is no higher than that of half the test samples in a group and no lower than that of the other half of the test samples in the group. The median value is frequently a more statistically useful measure of group performance than is the average or mean value of performance, especially if the values are not normally distributed (ESR is usually a log-normally distributed parameter).

Tables 2 through 4 contain data that are calculated from the data of Table 1. The intent of these tables is to highlight and precisely quantify the impact of selecting the superior material versus the conventional material for each of the three key types of material. For each type of material, the ESR improvement (reduction) generated by choosing the superior material is listed for each of the four possible combinations of the other two key materials. Positive numbers indicate that the superior material indeed produced superior performance (lower ESR) in the presence of a particular combination of the remaining two materials. Negative numbers indicate that the superior material produced inferior results. The right-most column of data in each table contains the average improvement generated in

the four test cells of each row by choosing the superior material. Perusing the right-most column of data, one can infer from the magnitude of the data which kinds of environmental stress highlight the benefits of choosing the superior materials over the conventional materials. Table 2 highlights the relative benefits of the superior carbon. Table 3 highlights the relative benefits of the superior silver paint Table 3 highlights the relative benefits of the superior metallic leadframe.

### ANALYSIS OF EXPERIMENTAL TEST DATA

The "as-manufactured" section of Table 1 demonstrates that the combination of all superior materials does, indeed, produce superior results. That is, the combination of the superior carbon, the superior silver paint, and the superior leadframe (far-right column in the "as-manufactured" section) produced the lowest median ESR (6.6 mΩ of any of the competing combinations. However many of the other combinations of superior and conventional materials produced very low ESR

Table 1 also contains median ESR data for each competing combination of materials after progressive exposure to each of the environmental stresses. Review of these data reveals that the combination of superior materials continues to have the best performance after each cumulative environmental stress. The superiority of this combination is particularly pronounced after 134 hours of HAST humidity testing and after 1000 hours at 175C. However many of the other combinations of superior and conventional materials produced substantially stable ESR in the face of many of the environmental stresses.

After cumulative exposure to all of the environmental stresses, the ESR of the capacitors manufactured with only superior key materials remains substantially stable while significant (and, sometimes, dramatic) ESR increases are observed for many of the other combinations of materials. The performance gap between the combination of all superior materials and the other competing combinations grows as the devices receive additional environmental stress. At the end of testing, the spread of performance among the competing combinations of material has widened by an amount that was unanticipated, and could not have easily been predicted based on the "as-manufactured" performance of this combination of superior materials. This points to a synergistic response among the superior materials when they are used in combination and are then exposed to severe environmental stress.

**TABLE 1.**

Median ESR (mΩ) of Capacitors Made with Superior and Conventional Carbon, Silver, and Leadframe

	<b>Carbon:</b>	<b>Conv.</b>	<b>Conv.</b>	<b>Conv.</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Sup.</b>	<b>Sup.</b>	<b>Sup.</b>
	<b>Silver:</b>	<b>Conv.</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Sup.</b>	<b>Conv.</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Sup.</b>
	<b>Leadframe:</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Conv.</b>	<b>Sup.</b>
<b>As Manufactured</b>		<b>10.4</b>	<b>7.7</b>	<b>9.2</b>	<b>6.8</b>	<b>10.0</b>	<b>7.5</b>	<b>8.7</b>	<b>6.6</b>
<b>Post 3 IR Reflows</b>		<b>12.8</b>	<b>11.6</b>	<b>9.9</b>	<b>6.9</b>	<b>13.3</b>	<b>9.4</b>	<b>8.8</b>	<b>6.4</b>
<b>Post 134 Hours Unbiased HAST</b>		<b>18.4</b>	<b>16.1</b>	<b>12.0</b>	<b>9.0</b>	<b>20.0</b>	<b>12.8</b>	<b>9.0</b>	<b>6.7</b>
<b>Post 500 Cycles Thermal Shock</b>		<b>16.1</b>	<b>13.0</b>	<b>11.9</b>	<b>8.7</b>	<b>15.3</b>	<b>10.3</b>	<b>9.6</b>	<b>6.9</b>
<b>Post 1000 Hours 150C Life, 0.5Vr</b>		<b>15.4</b>	<b>11.6</b>	<b>11.4</b>	<b>8.0</b>	<b>14.2</b>	<b>9.2</b>	<b>10.3</b>	<b>7.0</b>
<b>Post 1000 Hours 175C Life, 0.5Vr</b>		<b>40.6</b>	<b>36.8</b>	<b>33.6</b>	<b>26.7</b>	<b>14.6</b>	<b>9.9</b>	<b>12.1</b>	<b>8.2</b>

**TABLE 2.**

Reduction of 100 kHz ESR (mΩ) Due to Superior versus Conventional Carbon

	<b>Silver:</b>	<b>Conv.</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Sup.</b>	<b>Average of Row</b>
	<b>Leadframe:</b>	<b>Conv.</b>	<b>Sup.</b>	<b>Conv.</b>	<b>Sup.</b>	
<b>As Manufactured</b>		<b>0.4</b>	<b>0.2</b>	<b>0.5</b>	<b>0.2</b>	<b>0.3</b>
<b>Post 3 IR Reflows</b>		<b>-0.5</b>	<b>2.2</b>	<b>1.1</b>	<b>0.5</b>	<b>0.8</b>
<b>Post 134 Hours Unbiased HAST</b>		<b>-1.6</b>	<b>3.3</b>	<b>3.0</b>	<b>2.3</b>	<b>1.8</b>
<b>Post 500 Cycles Thermal Shock</b>		<b>0.8</b>	<b>2.7</b>	<b>2.3</b>	<b>1.8</b>	<b>1.9</b>
<b>Post 1000 Hours 150C Life, 0.5Vr</b>		<b>1.2</b>	<b>2.4</b>	<b>1.1</b>	<b>1.0</b>	<b>1.4</b>
<b>Post 1000 Hours 175C Life, 0.5Vr</b>		<b>24.0</b>	<b>26.9</b>	<b>21.5</b>	<b>18.5</b>	<b>22.7</b>

Tables 2 through 4 are derived from the data of Table 1 and each data value is a simple arithmetic difference between the two related data points in Table 1 (the data in the far-right columns are averages of these differences). These tables are provided to facilitate evaluation of the ESR improvements one achieves by using each superior material in combination with either superior or conventional versions of the remaining two

key materials. As previously stated, the impact of the superior carbon is highlighted in Table 2, the impact of the superior silver paint is highlighted in Table 3, and the impact of the superior metallic leadframe is highlighted in Table 4.

In the as-manufactured row of Table 2, the overall benefit derived from using the superior carbon with all

**TABLE 3.**

Reduction of 100 kHz ESR (mΩ) Due to Superior versus Conventional Silver

<b>Carbon: Leadframe:</b>	<b>Conv. Conv.</b>	<b>Conv. Sup.</b>	<b>Sup. Conv.</b>	<b>Sup. Sup.</b>	<b>Average of Row</b>
<b>As Manufactured</b>	1.2	0.9	1.3	0.9	1.1
<b>Post 3 IR Reflows</b>	2.9	4.7	4.5	3.0	3.8
<b>Post 134 Hours Unbiased HAST</b>	6.4	7.1	11.0	6.1	7.7
<b>Post 500 Cycles Thermal Shock</b>	4.2	4.3	5.7	3.4	4.4
<b>Post 1000 Hours 150C Life, 0.5Vr</b>	4.0	3.6	3.9	2.2	3.4
<b>Post 1000 Hours 175C Life, 0.5Vr</b>	7.0	10.1	2.5	1.7	5.3

**TABLE 4.**

Reduction of 100 kHz ESR (mΩ) Due to Superior versus Conventional Metallic Leadframe

<b>Silver: Leadframe:</b>	<b>Conv. Conv.</b>	<b>Conv. Sup.</b>	<b>Sup. Conv.</b>	<b>Sup. Sup.</b>	<b>Average of Row</b>
<b>As Manufactured</b>	2.7	2.4	2.5	2.1	2.4
<b>Post 3 IR Reflows</b>	1.2	3.0	3.9	2.4	2.6
<b>Post 134 Hours Unbiased HAST</b>	3.1	3.0	7.2	2.3	3.7
<b>Post 500 Cycles Thermal Shock</b>	3.1	3.2	8.0	2.7	4.3
<b>Post 1000 Hours 150C Life, 0.5Vr</b>	3.8	3.4	5.0	3.3	3.9
<b>Post 1000 Hours 175C Life, 0.5Vr</b>	3.8	6.9	4.7	3.9	4.8

combinations of silver paint and metallic leadframe is a 0.3 mΩ) reduction in ESR, a relatively small average improvement. However, the overall benefit of the superior carbon becomes more pronounced after cumulative environmental stress, where the most significant results are seen after 1000 hours at 175C. This indicates that the greatest contribution provided by the superior carbon is stability after lengthy exposure to very high temperatures.

Interestingly enough, using the superior carbon along with the combination of conventional silver paint and conventional leadframe actually results in a small deterioration of ESR performance after IR reflow and HAST exposure. Guided by these results, one might have been tempted to abandon the superior carbon had he not actually tested all of the combinations under all of the environmental stresses. Had the superior carbon been abandoned, then the remarkable performance

achieved from the use of all three superior materials in combination would never have been achieved.

In the “as-manufactured” row of Table 3, the overall benefit derived from using the superior silver paint with all combinations of carbon and metallic leadframe is a 1.1 mΩ reduction in ESR, a meaningful improvement. The overall benefit of the superior silver paint becomes more pronounced after cumulative environmental stress, where the most significant results are seen after 134 hours of HAST testing. This indicates that the greatest contribution provided by the superior silver paint is stability after exposure to intense moisture. The superior silver paint also makes a significant contribution to ESR stability after 1000 hours at 175C.

In the “as-manufactured” row of Table 4, the overall benefit derived from using the superior metallic leadframe with all combinations of carbon and silver paint is a 2.4 mΩ reduction in ESR, a substantial improvement. The overall benefit of the superior metallic leadframe becomes even more pronounced after cumulative environmental stress, where the most significant results are seen after 300 cycles of thermal shock and after 1000 hours at 175C. This indicates that the greatest contributions provided by the superior metallic leadframe are stability after rapid temperature changes and stability after lengthy exposure to very high temperatures.

Overall, the experimental data demonstrate that the best ESR performance is achieved when an three superior materials (and associated methods) are used in combination. Also, the data demonstrate that capacitors manufactured from these superior materials are remarkably more stable than capacitors manufactured from more conventional materials when the capacitors are exposed to severe environmental stress. Moreover, the data show that the beneficial effects of the superior materials may not be immediately obvious in the “as-manufactured” devices and that a full battery of environmental stresses must be applied to the devices to discover which stresses are best countered by each superior material.

### **OTHER ELECTRICAL PERFORMANCE DATA**

The previous discussion has focused primarily on the ESR performance of these devices, and, then, only on median performance of groups of devices. There is value in exploring other key electrical performance characteristics of these ultra-low ESR capacitors such as capacitance, dissipation factor, and DC leakage

current. Moreover, much can be learned from the statistical distribution of these parameters. That is, it is useful to know whether the superior key materials not only lower median ESR, but also whether their use leads to tight statistical distributions of ESR and of the other performance characteristics mentioned above.

Tight statistical distributions of key electrical characteristics (that remain within specification limits) and quality are often considered synonymous (e.g., six-sigma quality programs). Based on this premise, it should be possible to make an inference regarding the relative quality of the devices based on the statistical distribution of their electrical performance data. Also, absence of catastrophic failures and/or gross shifts of key electrical parameters (especially DC leakage) after severe cumulative environmental stress implies much about the expected reliability of these capacitors. That is, the more stable the device characteristics are, the more reliable the devices are likely to be, especially in harsh applications.

Graphs of the statistical distributions of four key electrical parameters appear in Figures 2 through 5. These electrical parameters are 100 kHz ESR, 120 Hz capacitance, 120 Hz dissipation factor, and DC leakage current at rated voltage. The format of the curves is either a normal or log-normal statistical plot. 120 Hz capacitance and dissipation factor tend to be normally distributed parameters while 100 kHz ESR and DC leakage current are typically log-normally distributed.

The term “normal” in normal and log-normal statistical plots refers to the scaling of the y-axis which is chosen to give a uniform spread of data points along the y-axis to data that are normally distributed with respect to the x-axis. The term “log” in log-normal statistical plots refers to the need for logarithmic scaling of the x-axis to uniformly spread the data points along the x-axis when data are log-normally distributed. In log-normally distributed data, the percentage difference between data points is normally distributed rather than the absolute difference. Linear scaling of the x-axis is used for normally distributed data.

Significant statistical information can be gathered from a glance at such plots. For example, the straighter the curve, the more the data fit either a normal or log-normal distribution (depending on the scaling of the x-axis as discussed above). Also, the more vertical the curve, the smaller is the standard deviation of the underlying statistical distribution. So, “perfect” curves would be straight vertical lines (all devices have identical performance). Moreover, if multiple curves

appear on such a plot, any differences in the statistical distributions of the underlying data sets can be immediately detected.

In the case of Figures 2 through 5, the multiple curves in each figure represent the selected electrical parameter after three IR reflows, after 134 hours of HAST humidity exposure, after 500 cycles of thermal shock, after 1000 hours of lifestesting at 150C, and after 1000 hours of lifestesting at 175C. These curves allow one to detect any shifts in electrical performance that are brought about by the cumulative effects of these environmental stresses. Also, the curves allow one to detect any shifts in the underlying statistical distributions.

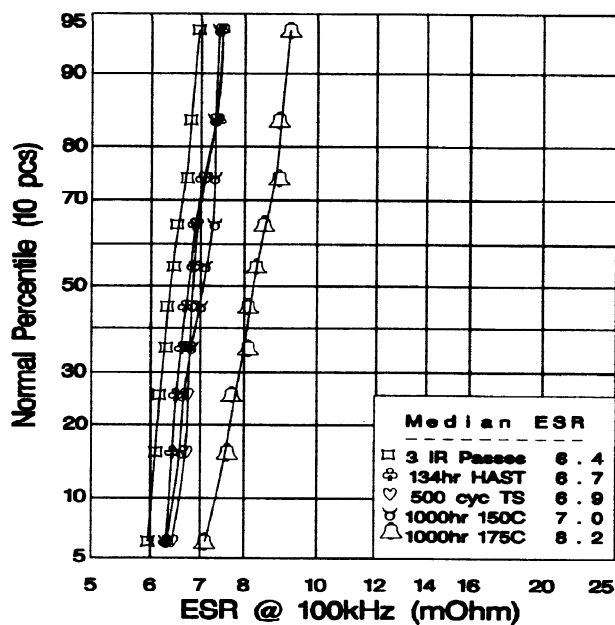


Figure 2. Log-Normal Statistical Graph of ESR of 1000 uF, 4v Capacitors after Exposure to Cumulative Environmental Stresses

Figure 2 contains the 100 kHz ESR data analyzed in the previous section for the capacitors manufactured from the combination of all three superior key materials. The median data reported previously are reported in the legend of the figure or may be determined by observing where the individual curves cross the 50% point on the y-axis. It is clear from the curves that the ESR data are, indeed, log-normally distributed (the data form almost straight lines) and that the standard deviation of the data points is small. Only after 1000 hours at 175C is there any substantial shift in the ESR of these devices, and, even then, the distribution of the data values (shape of the curve) is not significantly altered. Moreover, even after all of the cumulative

environmental stress, every ESR data point stayed below the “as-sold” catalog limit of 10 mΩ, demonstrating truly remarkable, rock-solid ESR stability.

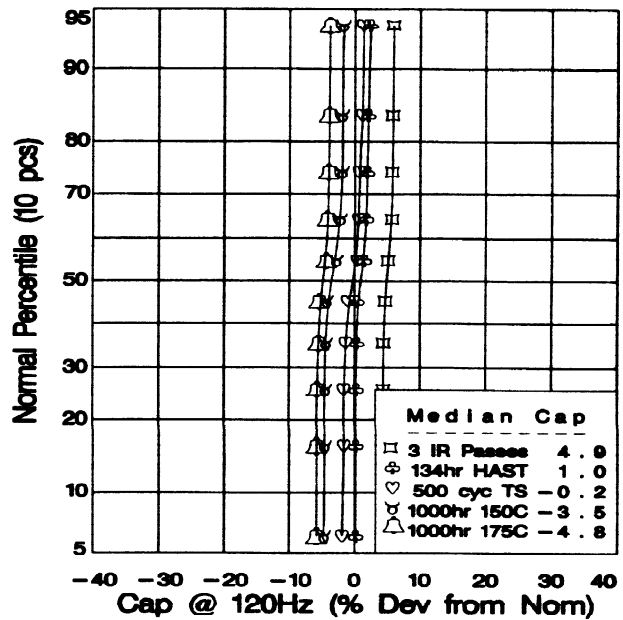


Figure 3. Normal Statistical Graph of Capacitance Percent Deviation from Nominal of 1000uF 4v Capacitors after Exposure to Cumulative Environmental Stresses

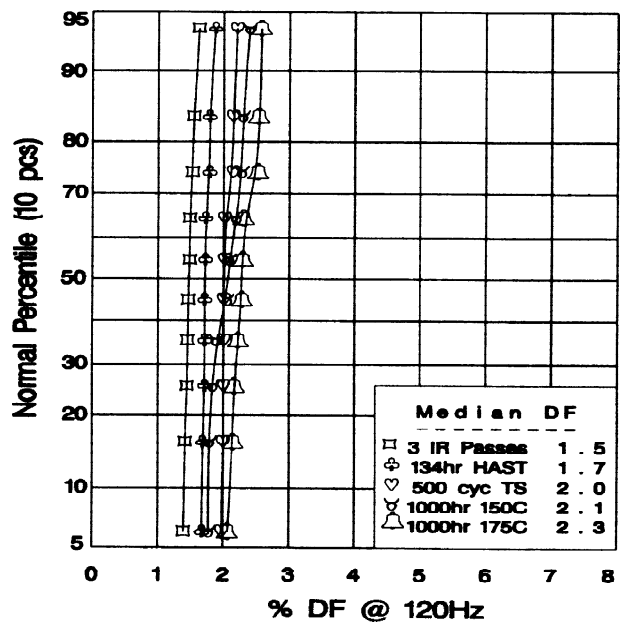


Figure 4. Normal Statistical Graph of Dissipation Factor of rooii, 4 V Capacitors after Exposure to Cumulative Environmental Stresses

Figures 3 and 4 contain 120 Hz capacitance and dissipation factor data for the capacitors manufactured from the combination of all three superior key materials. Even after severe cumulative environmental stress, only smooth, moderate shifts are observed with little or no substantial alteration of the underlying statistical distribution. Capacitance easily stayed within the “as-sold” capacitance tolerance of  $\pm 10\%$  of the nominal capacitance value, and the dissipation factor stayed well away from the “as-sold” catalog limit of 6%. A slight shift in the underlying distribution of the dissipation factor data is seen after 1000 hours of 150C life testing where some of the dissipation factor values actually improved. However, this shift does reflect an increase in the standard deviation of these data. The new, slightly-altered statistical distribution persists after 1000 hours of 175C life testing.

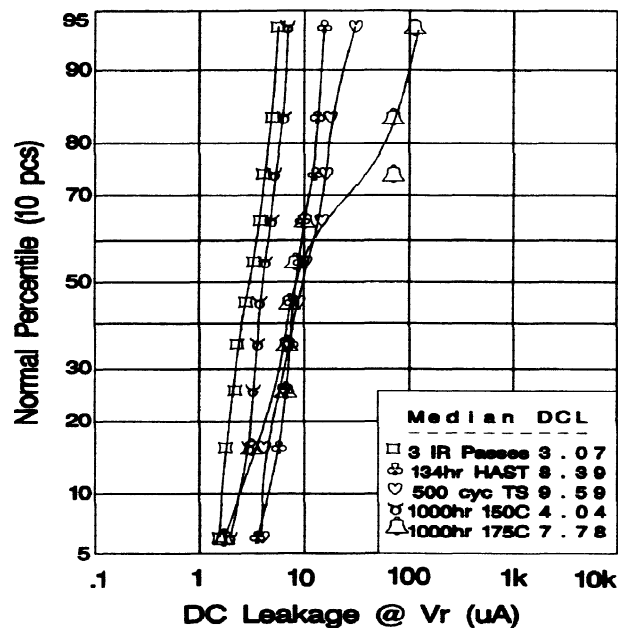


Figure 5. Log-Normal Statistical Graph of DC Leakage Current at Rated Voltage or 1000 uF, 4 v Capacitors after Exposure to Cumulative Environmental Stresses

DC leakage data for the capacitors manufactured from the combination of all three superior key materials appear in Figure 5. Several observations can be made from viewing these curves. First, through almost all of the cumulative environmental stresses, including 1000 hours of life testing at 150C, the DC leakage current remained below the “as-sold” catalog limit of 40 uA. Only after an additional 1000 hours of life test at 175C did a few of the capacitors exceed their initial catalog limit. Moreover, these higher DC leakage readings for several of the devices were, to some degree, balanced by

reductions in DC leakage in other devices. Finally, even though several of the devices showed increased DC leakage after 1000 hours of life test at 175C, these increases were moderate and stable. There were no catastrophic failures observed even under this most-extreme dose of environmental stress.

### OBSERVATIONS AND CONCLUSIONS

The data presented here support several observations and conclusions. First, that it is possible to manufacture ultra-low ESR tantalum chip capacitors without sacrificing product quality and reliability. The environmental stresses employed to test these new devices are, generally, in excess of what most capacitors would experience during in-house manufacturer testing or during customer use. Moreover, the stresses were applied cumulatively, a testing regime that is even more harsh, and not commonly employed. These are remarkably tough and stable devices, and they should broaden the scope of potential applications that one would consider for tantalum chip capacitors.

Second, surprises still happen in the product-development process. When the superior carbon was applied in combination with the conventional silver paint and leadframe, ESR actually deteriorated slightly after 3 IR reflows and HAST testing. Had the test program not been thorough, the benefits afforded by the superior carbon in combination with either the superior silver paint and/or the superior leadframe might not have been achieved. Moreover, excessive ESR increases above 150C would have limited the ultimate performance of these new capacitors by a significant margin. Along the same vein, if only “as-manufactured” ESR performance had been tested, one might not have bothered to explore all combinations of materials since many combinations of only one or two superior materials easily produced ESR below the desired 10 mΩ level.

Finally, the task of ESR reduction is not yet finished. Ever-lower ESR requirements will arise as processor power supply voltages fall and processor currents rise. Manufacturing a 5 mΩ tantalum chip capacitor is, obviously, the next challenge. What new changes in materials, processes, and/or configuration will facilitate the accomplishment of this goal? Stay tuned, there are more exciting developments to come.

## **REFERNCES**

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