

KEMET Electronics Corp.

Voltage Coefficients Rob Capacitance

The High CV product available with MLC surface mount chips today is truly impressive. With the ceramic's inherently low ESR, these devices appear to be a near ideal device for today's demanding low voltage power supply output filter and microprocessor decoupling needs. Yet, there are characteristics of the MLC device that need to be fully understood in order to prevent problems that may be created with these devices. The major consideration that needs to be understood are the DC and AC voltage coefficient properties with these devices.

The voltage coefficients must be analyzed within DC and AC modes as these may appear to be conflicting elements. With DC bias, the dielectric constant of the ceramic appears to decrease with increasing magnitudes of bias. With AC signal levels, the capacitance appears to decay with decreasing magnitudes of AC voltages. The required capacitance (nameplate capacitance) is verified by the manufacturer with a low frequency AC signal, while there is no DC bias applied.

The effects of DC bias were initially controlled in some military specifications by defining the BX (-25% max deviation over temperature with 100% applied voltage) and BR (-40%) characteristics within the Voltage/Temperature Coefficients (VTC) of the part. In the commercial world, these characteristics are totally open. In Figure 1, the change in capacitance versus the applied DC voltage is plotted. There are two other manufacturers plotted along with KEMET's capacitors, as these are high capacitance, low voltage X5R dielectric devices. The response shows that at 1/2 rated voltage, the loss of capacitance is in excess of 30% from the initial value at 0 VDC.

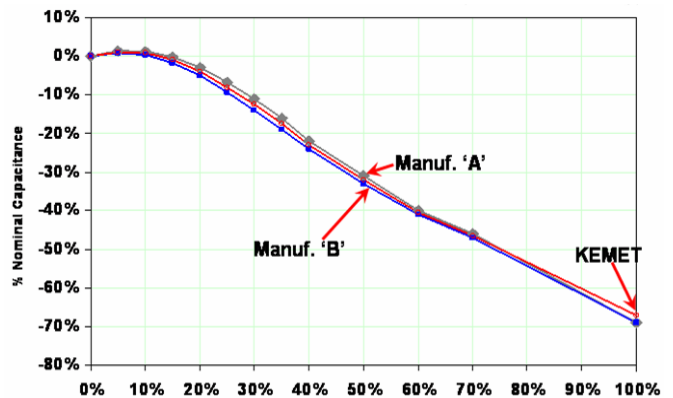


Figure 1. Loss of capacitance due to DC bias effects.

Of equal importance is the AC voltage effect. Prior to

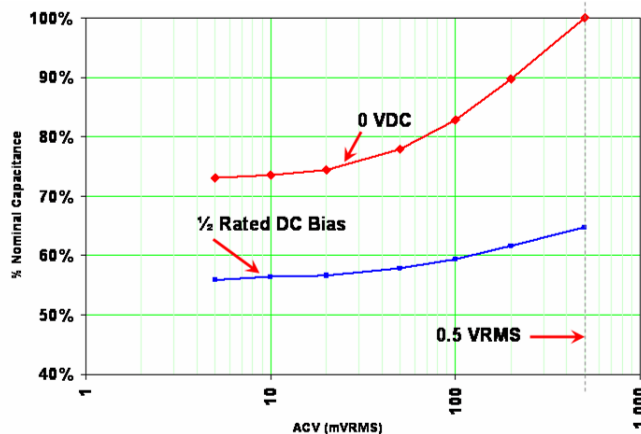


Figure 2. Loss of capacitance at AC voltages less than 0.5 VRMS.

the larger capacitance values recently achieved, the requirement for measuring capacitance was at 1.0 VRMS and at 1 kHz. This developed into a problem because the oscillators in the test equipment could not maintain that voltage for capacitance larger than 10 uF, as the lower impedance created higher currents to maintain that 1.0 VRMS signal. The capacitor industry settled on the 0.5 VRMS at 120 Hz measurement as a new standard for MLC capacitance values above 10 uF. As the final circuit application moves to higher frequencies and lower voltages, the capacitance apparent to the circuit is diminished. The effects of the AC magnitude are shown in Figure 2, with the 0.5 VRMS denoted in this response. In many actual applications, this magnitude of AC voltage would indicate the circuit is not working because typical maximum voltages should range more between 10 mV and 5 mV, and at much higher frequencies.

Compound this AC voltage effect with the DC bias effects and the blue line (or bottom line) of Figure 2, points to a capacitance loss of over 40% could be apparent for these combined effects.

Finally, consider the frequency of measurement as opposed to the frequency of application: the measurements being made at 120 Hz and the applications are at 100 kHz, at minimum. There is a slight decay of dielectric constant between these two frequency points that may create a 15% loss of capacitance, at most.

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