ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications

Tanmoy Roy, Larry Smith

Sun Microsystems, Inc., MS MPK15-103
901 San Antonio Rd.,Palo Alto, CA 94303-4900.
tanmoy.roy@eng.sun.com, Fax: (650) 786 6457

John Prymak

Kemet Electronic Corporation
P.O. Box 5928, Greenville, SC 29606.
johnprymak@kemet.com

ABSTRACT

Power distribution system noise affects computer product timing performance, signal integrity and electromagnetic interference. Between 1 MHz and 1 GHz, the primary means of reducing power distribution noise is with ceramic decoupling capacitors. To achieve a certain target impedance, it is important to characterize the ESR of ceramic decoupling capacitors as they directly determine the number of capacitors required on a board. A new technique to extract ESR is described in this paper. Another factor which determines the capacitance value of decoupling capacitors is the ESL (inductance) associated with capacitors mounted on a PCB. A study that compares the ESL of different pad layout geometries will also be presented.

I. Introduction

There are various design issues which affect the power distribution impedance. It has already been demonstrated that the power distribution impedance for a modern computer must be kept low and flat over a large frequency range [1] for improved product performance. A typical switching regulator maintains a low impedance up to 30KHz. Above that, bulk capacitance provides the low impedance up to 1MHz. High frequency decoupling is provided by ceramic capacitors up to several hundred MHz. Ceramic capacitors reach their minimum impedance (ESR) at their resonant frequency, which is determined by the capacitance and ESL. To meet a target impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have an impedance that is equal to it's ESR. Then, a sufficient number of those capacitors are placed in parallel so that the parallel ESR's approach the desired target impedance.

Most of the inductance associated with a decoupling capacitor is due to the mounting pad structure. Inductance is minimized by moving Vdd and Gnd vias close to each other and minimizing the length of via from the pad to the power planes. Careful pad layout design (low inductance) enables the use of higher value capacitors for the same frequency. Larger value capacitors generally have a lower ESR, so fewer of them are required to meet a target impedance.

Capacitor ESR determines the number of capacitors required to achieve a certain target impedance at a particular frequency and is therefore an important design parameter. The ESR value typically reported by capacitor vendors underestimates the actual ESR of a capacitor mounted on a PCB. A novel technique for measuring ESR involving soldered down capacitors is described in this paper. This measurement technique accurately reflects actual performance of capacitors soldered onto PCB's. The

current industry technique of using a surface mount device (SMD) test fixture to measure ESR under estimates the actual ESR if compensation techniques are used.

II. ESL Contribution

The mounted inductance or ESL of a capacitor is comprised of three components: pad layout, capacitor height and power plane spreading inductance. These three elements describe the loop that current must flow within. The bigger the loop, the more the inductance. The pad layout for a capacitor dominates the ESL. It consists of via placement with respect to the pad, the length and width of traces connected to the pad, and the way the vias are connected to the power and Gnd planes. The location of the power/Gnd planes in the PCB stackup controls the height of the via which is major contributor to pad inductance. If we observe the magnetic field on a plane parallel to the pads but below the pads, most of the energy is concentrated between two vias and negligible outside them. Inductance directly depends on the magnetic field, so reducing the energy associated with the magnetic field reduces overall inductance. This reduction is achieved by reducing the size of the current loop. Figure 1 shows a comparative study of various pad layout designs.

In the earlier design, the placement of vias were random and based on convenient layout of the board. Long traces were connected to the pads and the inductance was very high. As we move the vias to the back of the pads, closer to the edge, we see a significant reduction in inductance. Finally moving the vias to the broadside we reach a optimum location where the layout meets all design and manufacturing ground rules. The inductance can be further reduced by placing vias in the pads, which is under investigation for manufacturing feasibility. For this chart, the length of all vias (determined by the PCB stackup) was 62 mils.

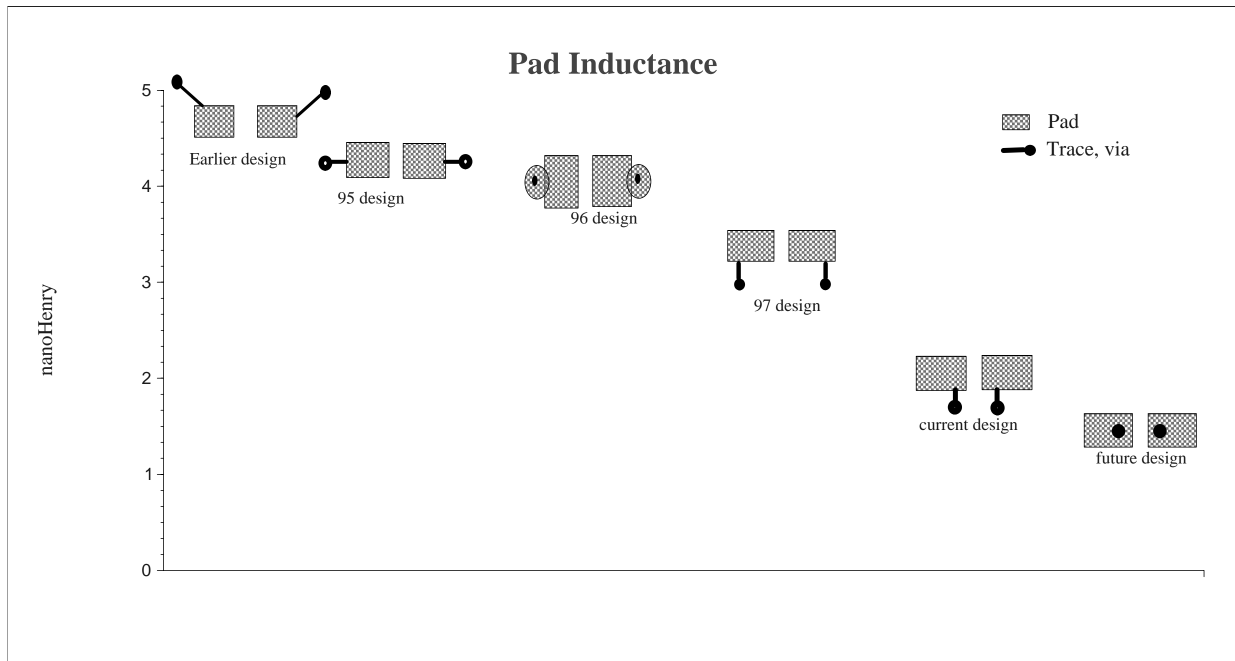

Fig 1. Inductance due to various pad layouts.

The second contributing factor to the inductance is the capacitor itself. The capacitor forms a part of the current loop, hence contributes to the inductance. Typically a capacitor is made of multiple plates connected alternately to the side posts. For a thicker capacitor, the current has to flow up and down and effectively increases the length of the current loop. Inductance due to the capacitor is determined by the capacitance value and the vendor. Typically a capacitor of thickness 40 mils (0805 size) contributes 400pH of inductance.

The inductance associated with current spreading into the power/Gnd planes also contributes to the total mounted inductance. Current in the planes becomes concentrated in the vicinity of the vias. Concentrated current creates a higher magnetic field and therefor contributes to inductance. Spreading inductance is higher at the edges and corners of the PCB. Current can approach vias in the middle of the board from four different directions instead of two when the capacitor is located at the corner of the board. Also the separation between the planes contributes to the spreading inductance. Figure 2 shows the spreading inductance for different board locations for various plane separations. It is clear that inductance is higher at the corner of the board compared to edges and the center of the board. Therefore spreading inductance is minimized by keeping power planes close to each other. By careful pad design and reducing the plane separation a 7x improvement in inductance can be achieved.

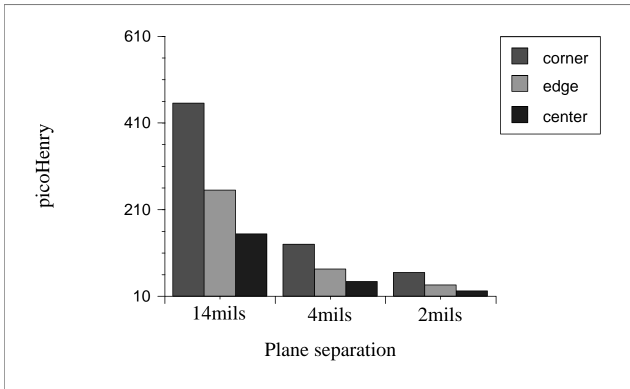

Figure 2. Spreading Inductance due to power planes.

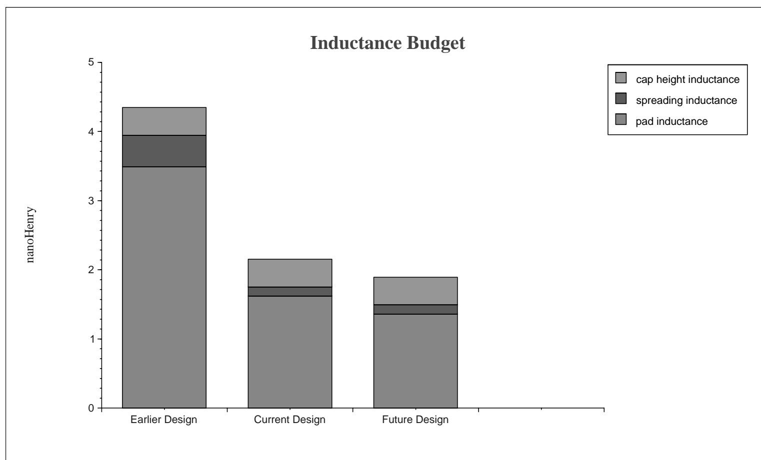

Figure 3. Total Inductance comparison.

The relative importance of pad layout, spreading inductance and capacitor height is compared in figure 3. Pad layout dominates inductance. By careful pad layout and by minimizing power plane separation, the ESL of decoupling capacitors can be cut in half.

III. ESR Estimation

The power distribution impedance should be kept at or below a target impedance across a broad frequency range. Ceramic capacitors are the means of doing that between 1 MHz and several hundred MHz. ESR determines a capacitor's minimum impedance so it is important to characterize it correctly. An over estimate of ESR leads to too many capacitors and unnecessary expense. An underestimate of ESR can lead to an inadequate power distribution system.

The traditional ESR measurement technique using HP4291A Impedance Analyzer uses a surface mount test fixture. The chip capacitors are placed on the surface of the electrodes and spring action is used to keep a contact pressure. The setup is calibrated and compensated using a small conductive block of material before actual measurements are made. In the calibration and compensation process, an attempt is made to compensate for the contact resistance. It is not possible to distinguish between contact resistance and capacitor ESR. Unfortunately, the compensation process often compensates out the very thing that is being measured. It was found that the measurement done this way under estimates the actual ESR value.

A better measurement technique is based on a low impedance test head connected to an Impedance Analyzer. An SMA connector is connected to the test head through an APC-7 connector. Calibration is performed at the end of the SMA connector. The capacitor chip is placed on the SMA connector and soldered down. Measurements have been made on X7R and NPO dielectric capacitors. Data has been collected for different size capacitors (0603,0805,1206).

The collected data is used for a Linear Regression model (Log(mΩ) vs pF) and the projected curves are plotted in fig. 4. The capacitors measured are of values from 22pF-10µF. The ESR measured using this technique is 2-3x times higher than the ESR measured by the standard industry technique involving an SMD fixture. Soldered down capacitors represent the true behavior of capacitors soldered onto a PCB.

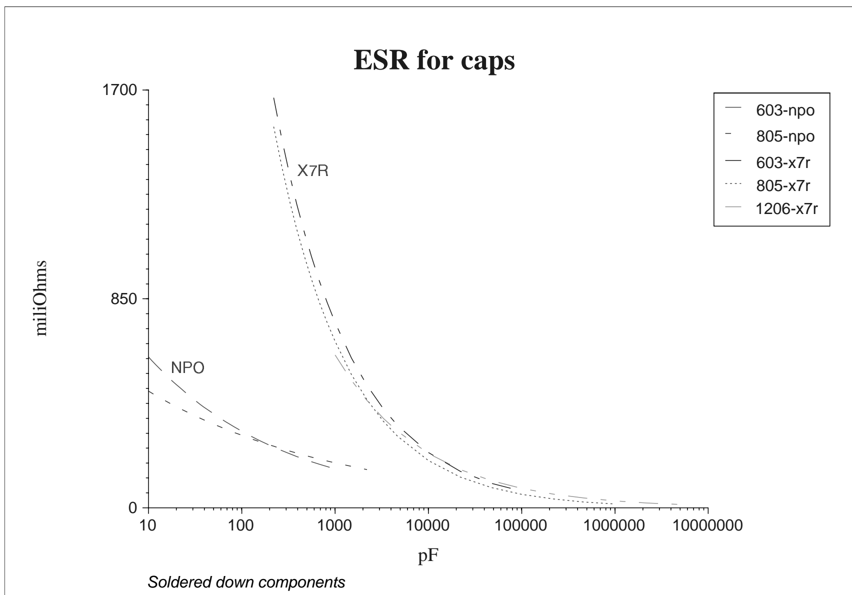

Fig 4. ESR values for various caps.

IV. Conclusion

The ESL (mounted inductance) and ESR of a capacitor are the two major factors to be considered when designing a power distribution system. The pad layout is the largest contributor to ESL and can be controlled by careful design of vias and power planes. Spreading inductance can be reduced by placing the power and Gnd planes close to each other. A novel technique for ESR estimation is presented which better represents it's true value on a digital board. The industry standard technique using an SMD test fixture gives an ESR value that is 1/2 to 1/3 of the real ESR.

V. References

[1] L. Smith, "Decoupling Capacitor Calculations for CMOS Circuits," Electrical Performance of Electronic Packaging Conference, Nov. 1994.