**TecForum TF-MP2**

**Inductance of Bypass Capacitors**

**How to Define, How to Measure, How to Simulate**

**Presenters:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Organization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Joseph M. Hock</td>
<td>AVX Advanced Product and Technology Center</td>
</tr>
<tr>
<td>John D. Prymak</td>
<td>KEMET Electronics Corp.</td>
</tr>
<tr>
<td>Steve Weir</td>
<td>Teraspeed Consulting Group</td>
</tr>
<tr>
<td>Mark Alexander</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>Istvan Novak</td>
<td>SUN Microsystems, Inc.</td>
</tr>
</tbody>
</table>

**Session organizer and chair:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Organization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Istvan Novak</td>
<td>SUN Microsystems, Inc.</td>
</tr>
</tbody>
</table>

**Abstract**

Have you ever wondered why the same size bypass capacitor is listed with different inductance from different vendors? Do you want to know how some of the major OEMs want the inductance to be determined? Are you interested in knowing how major capacitor vendors measure the inductance? This TecForum will give an overview of how OEMs (Xilinx, SUN) model capacitors, what are the important contributors to a capacitor's inductance in a real design, as well as how capacitor vendors (AVX, Kemet) do the testing. Participants who want a dialog with the presenters, can attend the panel discussion "Bypass capacitors: how to determine their inductance?"

This is a continuation of the TecForum and panel discussions at DesignCon 2005, Santa Clara, on the same topic held by Sanyo, Taiyo-Yuden, Cisco, Intel and SUN.
Part II. Designing and Measuring Low ESL in Capacitors

John D. Prymak, KEMET Electronics Corp.
PO Box 5928, Greenville, SC 29650
Phone: (864) 963-6300 / FAX: (864) 967-6876, Email: johnprymak@kemet.com
John has been working for KEMET the past 15 years in technology and technical marketing departments. He worked for AVX, another capacitor manufacturer, for the previous 15 years, starting out as a technician and leaving as Product Development Manager. John has authored and co-authored many technical papers presented at CARTS, APEC, ECTC, and other technical symposiums, covering failure analysis, flex, surge, EMI/RFI, electrical performance, ESR, ESL, and is author of the KEMET Spice software.

Mike Prevallet, KEMET Electronics Corp.
PO Box 5928, Greenville, SC 29650
Phone: (864) 963-6300 / FAX: (864) 963-6521, Email: mikeprevallet@kemet.com
Mike has been with KEMET for over ten years. He is a licensed professional engineer in the state of South Carolina, and holds a bachelor's degree in electrical engineering from Clemson University and a master's degree from the University of South Carolina. His current position is Applications Manager.

Peter Blais, KEMET Electronics Corp.
66 Concord Street, Suite Z, Wilmington, MA 01887-2127
Phone: (978) 658-1663 ext 226
FAX: (978) 658-1790, Email: peterblais@kemet.com
Peter is engaged in providing design and technical support to key KEMET customers and product direction based on market input. He has over 20 years of experience in the technology industry including positions as Director of North American Sales, LinkUp Systems and Regional Sales Manager, Murata Electronics, N.A. Mr. Blais holds a B.S.E.E. from Rensselaer Polytechnic Institute.

Abstract
A great deal of discussion has taken place at these conferences detailing the techniques and problems in measuring the effective series inductance (ESL) in low inductance capacitors. The most universal method utilizes a network analyzer and the test capacitor mounted as a parallel device in the source-analyzer coaxial line. There are other methods used for this analysis and we will discuss one here. Additionally, the ESL property is normally assumed to be a constant, but we will introduce evidence to show that this parasitic, like its companion parasitic, ESR (effective series resistance), may be changing with frequency. Although discussion of low inductance might appear to be the realm of multilayer ceramic capacitors, we will also detail a surface mount electrolytic capacitor as a low ESL product.
Defining ESL

Discussions about inductance in a capacitor may seem analogous to discussions about screen doors on submarines, but unlike the latter, the former does exist. Any time the current path is defined with a limited directional length, inductance will occur. In most two-terminal devices, the path exists within the structure or body of the device, from terminal A to terminal B. It is a force that is analogous to inertia in a mechanical system. Once a body is at rest, it tends to stay at rest and once a body is in motion, it tends to stay in motion. With inductance, the ‘body’ is current, and once a current level is achieved (as no current in an “off” state or as sustained current in an “on” state) the current desires to stay at those levels. The sustaining element in this current is the magnetic fields associated with the current and changing the current requires changing the magnetic fields associated with it.

The dimensional aspects of the capacitor may have a huge impact on its effective series inductance (ESL) and also contribute to the effective series resistance (ESR) of the capacitor. As the ESR was continually decreased, the application frequencies moved higher until ESL began to dominate the problems associated with high frequency decoupling and power filtering.

The Two-Terminal Capacitor

The capacitor has evolved from a leaded device to a surface-mount device and, as its simplest diagram might predict, as a two-terminal device. The terminals may be found at opposing faces of the element as in axial leaded devices, or along a common face as in radial leaded devices. Although it is readily seen that the leads associated with through-hole devices add length and, therefore, inductance to the leaded capacitors, this increased path length is eliminated with the surface mount chip capacitor.

The inductance in any device, be it a conductor, resistor, or capacitor, is determined by the restriction in the width of the device established over the duration of its length. The higher the restriction is (narrower the length) the higher the inductance becomes and, the longer the duration is, the higher the inductance becomes. Consider a capacitor that is long and narrow: the path is defined over a long distance and a narrowly constrained path. This type of capacitor would have a high inductance associated with the dimensions of its structure. If the path was to be made short and wide, both the restraint and the duration is decreased, thus the inductance is decreased.

Manipulating these effects for lower ESL would require that the capacitor be built as short as possible and as wide as possible. These devices are represented in the “reverse geometry,” low inductance MLC (multi-layer ceramic) capacitor offerings. The 1206 chip becomes the 0612 chip (1206 is 0.120 in. by 0.60 in. and 0612 is 0.060 in. by 0.120 in.). This transposition results in decreasing the ESL by nearly 50%. This manipulation in manufacturing is not without added costs since processing these MLC capacitors is through equipment optimized to handle the traditional devices that are long and narrow, as opposed to being short and wide.

Figure 1. ESL can be improved with shorter and wider current path in the device.
The aspect ratio limitation

There is a limitation to how low of an inductance can be achieved with the reverse geometry approach. If we consider the aspect ratio (AR) of the device as the ratio of the length divided by the width, the aspect ratio for the reverse geometry part previously discussed goes from 2 to 0.5 (1206 to 0612). Using the effects established with that conversion, it follows that the reduction of 50% in ESL should decay another 50% for each halving of the aspect ratio.

Limitation of lower AR

Lower AR reduces plate L.

Optimum AR ~ 0.2
Optimum ESL ~ 150 pH

Figure 2. Improvement in ESL is not continuous with decreasing aspect ratios\[^2\].

The problem is that this effect appears to no longer continue once the aspect ratio gets below 0.2 and this diminishing effect may be due to the charge concentrations. On each electrode plate, there is an unequal distribution of charge within the plate area. The peak concentration of charge will appear at the corners of the plate, along the edge that is opposite the termination edge. As the aspect ratio goes from 0.5 to 0.2, the charge concentrations on each plate may extend further into the center of the edge opposite the termination, allowing the charge and discharge current paths to extend to wider segments of the termination edge. As the aspect ratio goes lower still, the concentrations may cease to increase along the edge opposite the termination at the same rate as the changing aspect ratios above the 0.2 level. The current paths again may grow wider, but at diminished rates.

Charge Concentration

Charge concentrations in corners opposite plate termination edge.

Dominant Current Path

Figure 3. Declines in ESL with reduced aspect ratios may be due to effects on charge concentrations.

This effect may also be factored by measurement capabilities. For aspect ratios below 0.2, the calibration of the fixtures and the boards could have been misleading, but in all of our attempts to eliminate these influences, we were unable to see the continuing improvement with reduced aspect ratios.
The best capability we could measure for the reverse geometry devices was in the range of 150 to 200 pF. Mounting these on the PCB presented additional ESL as feed lines (traces) or vias to these capacitors from the power and ground planes added to the inductance apparent to the overall circuit.

**Multi-Terminal Devices**

These variations of the two-terminal devices allowed MLC capacitors to achieve ESL levels below 200 pF, but were limited there. Consider that the plate charge as depicted in Figure 3, required that the majority of the charge to travel from the termination edge of the electrode plate to the opposite edge of the plate and that the adjacent plates are terminated at opposing faces in the two-terminal capacitor. One plate is charging, and the plates immediately adjacent to it are discharging. The net effect is that the charges are moving in the same direction. Looking at the MLC structure, the initial logic might be that if these plates are inductive, then connecting inductive plates in parallel should create an effect similar to resistors in parallel: as more plates are added, the net ESL of the capacitor should decrease.

The laws of inductors in parallel do invoke a similar principle, but with the caveat that these inductors do not have any magnetic links to each other. These plates are separated by microns or fractions of microns and they do have a magnetic influence on each other (referred to as mutual inductance). This effect shows that, based on the self-resonance frequency, as the capacitance increases with increasing layer counts, the determined ESL (based on capacitance and self-resonance) also increases.

![Mutual Inductance](image)

**Figure 4.** The ceramic MLC contains self-inductance of plates, and mutual inductance by association.

![Two-Terminal / Same Face](image)

**Figure 5.** Here is a two-terminal capacitor with the terminations on the same face.

In order to reduce this effect, opposing terminations on the same face of the capacitor may be created. In this device as shown in Figure 5, the adjacent (oppositely charges) plates ‘A’ and ‘B’ are terminated along the same edge with each successive layer of ceramic. The terminations for these plates, ‘A’ and ‘B’ respectively, will appear along the same face of the ceramic block, once all the layers are stacked and the unit is fired. This arrangement will create some inductive cancellation since the charges on these two plates are moving in opposite directions, allowing the magnetic fields to cancel rather than reinforce each other.

This structure would require the capacitor to be of sufficient height (the dimension along the vertical axis of the drawing in Figure 5) to allow the current to spread out from the neck-down termination edge at the bottom edge to create the cancellation effects. In this instance, the ESL will improve compared to a two terminal device, but the ESR will increase due to the loss of contact length along the termination edge.
Now we referred to the vertical axis in Figure 5 as the “height” dimension, but that does not restrict this device to a board mount where the height is perpendicular to the plane of the board. Rather than sticking up from the board, it may be laid down such that the ‘A’ and ‘B’ terminations are arranged to be on a face that is perpendicular to the board, with allowance for both termination ‘A’ and ‘B’ to be mounted to adjacent solder pads on the board. In this case, the wrap around effects of the external terminations would allow this device to be mounted to the pads through the wrap-under termination. This presents an opportunity for adding more terminations along the other vertical faces of the capacitor body. These terminations could be repeated along the entire perimeter of the body - allowing for this sequence to be repeated a number of times, creating an interdigitated termination scheme for the device. This interdigitated capacitor (IDC) scheme changes the charge distribution on the plate structure. As illustrated in Figure 6, the effect of feeding charge from opposing edges of the plate is that the charge concentrations to the opposing edge do not have to come from the terminals on opposite edges. For the two terminals at the top of the illustration, the adjacent edge along the top is also the opposing edge for the terminals along the bottom. The charges do not have to travel across the plate dimensions, thereby reducing the duration of the path. This results in reductions in both the ESL and the ESR. Also, consider that as the charge comes into the plate, it immediately fans out in opposing directions to fill the charge requirements along the feed edge (Figure 7). Charges moving in opposite directions create fields that interfere with each other, instead of reinforcing each other. The termination edges are repeated at multiple points, therefore eliminating the negative impact on resistance as attributed to the device in Figure 5.

*Figure 6. The charge concentration on each plate of the IDC is to the outer perimeter of the plate[^3].*

*Figure 7. Charge movement within and into the IDC in opposing directions, adheres to cancellation goals[^1].*

Also, the terminations shown are for one plate. The adjacent plate would have terminations that would be directly across the chip, fitting in between those shown. The perimeter would create an A-B-A-B termination sequence along the top of the chip (left to right), repeated in a circular pattern around the center of the chip to another A-B-A-B sequence at the bottom of the chip (right to left). As illustrated in Figure 7, this presents another opportunity for inductive cancellation, as the feed of charge through the adjacent terminations is in opposing directions.

**The Low ESL Conductive Polymer Capacitor**

There are other methods used in attempts to minimize the ESL in MLC capacitors that cannot be pursued in this paper. The IDC is the dominant low ESL package that is gaining widespread acceptance and usage. The creation of the low ESL devices in the MLC package grows out of the high adaptability of its structure to these geometric variations of the package and termination designs that makes it so readily manipulated.
The adaptability of the conductive polymer capacitor is not as open as the MLC mainly because of its anodized pellet structure. In the process of creating the dielectric as an oxide of the base metal pellet structure. The anodization process restricts the feeds into the pellet structure to the same singular anode contact, though the contact to the cathode may appear on multiple faces. There are methods of multiple feeds being researched, but today, these are not production ready. As such, this device is pretty much restricted to the two-terminal device; but there are several things we can do to lower the ESL.

Consider the two terminal capacitor and the effects created with the reverse geometry structure. Again, the conductive polymer capacitor does not lend itself to changing from a 7343 to a 4373, because of the anodization requirements. This device is packaged in plastic (injection mold process) and a leadframe is used to bring electrical connection from the capacitor’s pellet structure out to a high-speed, pick-and-place plastic package for surface mount applications. That leadframe adds a lot of length (duration) to the current path for this device (Figure 8). At the anode connection, the leadframe extends from the middle of the package where it contacts the riser wire to the outside face of the plastic package where it is then bent down and under the end of the plastic body. At the bottom face of the device, this leadframe makes contact with the solder pad on the PCB. The cathode connection starts along the top of the pellet, is bent down to the middle of the plastic body, then out, down, and under to repeat the solder pad contact. There is a lot of wasted volume created in this design. To be honest, it was that loss of capacitance volume that guided the development of the design without the leadframe. This loss becomes a greater percentage of the package volume as the chip size is reduced. In order to reclaim some of that lost volume the facedown design was created.

**ESL Components – SMD Conductive Polymer**

Anode current paths are mostly dispersive - minor contributor.

Riser-Wire round conductor

Leadframe rectangular conductor

Figure 8. Here is a standard, surface mount conductive polymer capacitor[2].

**Reduced ESL Loop Areas**

Conductive-Polymer STD Chip
Conductive-Polymer Face-Down Chip

Figure 9. Illustration of reduced current loops afforded by facedown design.
The facedown terminations did allow us to recover that volume, but it was noted that it also created a lower ESL in the component. The reasons are the obvious loss of the leadframe’s added length (duration) to the current paths. Looking at this effect as reduced current path loop area is illustrated in Figure 9.

The facedown termination pads created with the device on the right of Figure 9 are in immediate contact with the cathode surface of the pellet structure and the anode plate is contacted through a conductive spacer. The results of the conversion of the “T” case (3528-12) device resulted in a drop in ESL of over 50%. Again, this change was not to optimize ESL, but to increase volumetric efficiency. As a matter of fact, the space separating the anode and cathode termination plates was kept large to assure that this device could be mounted using existing “T” case solder pads.

Looking purely at optimizing the ESL, there was a benchmark already in the market – the Sanyo TPL series[3]. This device is a three-terminal, conductive polymer based device with an ESL in the range of 520 pH. The key to this device is the separation space of the anode and cathode contacts at 1.10 mm. The third termination, internally connected to the middle termination, is created for mechanical stability and solder balance.

Our facedown 7343 has only two terminals for electrical contact to the board, but we will recommend that the users use three solder pads (same as Sanyo TPL) for solder balance. The bottom surfaces of the termination plates are tin plated over nickel plating. The ESL is in the range of 520 pH. The height of the chip will be at 1.5 mm, 1.7 mm, and 1.9 mm maximums.

![Figure 10. Here is the outline for the 7343FD, low inductance conductive polymer capacitor.](image)

The recommended solder pads are shown in Figure 11 and there are three pads instead of only two. The reason for this is that if the cathode contact were one, large pad, then the mass of solder created between the solder pad and the termination plate may be large enough to draw together and lift the capacitor, possibly lifting the anode contact away from its pad. By splitting the solder pads into two smaller areas, there will be a smaller mass of solder thus eliminating this.
Measuring the parasitics

The movement to eliminate the parasitics in capacitors has followed a sequential pattern. The initial attempts were to reduce ESR, as this was perceived to be the main debilitating factor in circuit response. The measurement of ESL could be obtained in one of two methods. The first is to measure the self-resonance of the capacitor and, based on the formula for the resonance of a series LC circuit, the inductive element could easily be deduced. The second method was to measure the impedance of the device at a frequency well above the self-resonance of the capacitor and, assuming that this impedance was dominated by the ESL element of the capacitor, the magnitude of the reactive element of the impedance was assumed to be the inductive reactance of the ESL at that frequency.

In most instances with MLC capacitors, this can result in different levels of ESL – a high ESL at self-resonance, and a lower ESL at frequencies well above self-resonance. We believe that this difference is attributable to the current being restricted to the lower plates in the frequencies above self-resonance, while the current involves more plates at self-resonance. The effect can be seen as detailed in Figure 12.

ESL changes with Frequency

Figure 12. Two distinct ESLs are apparent if measuring at self-resonance and well above this frequency.
The added impedance in getting the currents into the higher plates is due to the added resistance and inductance created by the vertical elements of the terminations as they rise above the board to connect the upper electrodes. Eventually, all capacitors of the same design (e.g., 0603 or 0805) have their currents defined by the smaller loop – and they all appear to have the same ESL.

We do not believe this transition to be a step function, but a gradual effect. We plan on incorporating this effect in the KEMET Spice models, but we are trying to see if we can define the transition in a clearer manner.

**Network Analyzer**

From previous reports presented at this and other conference, we think that the work in this area has been excellent. We are concerned with one aspect that has been touched on lightly, and that is standardization. The geometries of the mounting fixtures are paramount to universal replication. There needs to be a standards committee taking this up. At one time, the EIA was trying to put a standard together, but we have not heard of any developments.

One more complaint: Following the practices that were beaten on us though our science classes, our results were always to be within the significant figures measured. Today, the readings may be flashed up on a screen as 200.015 pH. Does this system truly have a resolution of 0.001 pH? (That is 1 fH.) Repeat the reading, without moving the piece, immediately after the first reading and the reading now is displayed as 200.356 pH. Is the inductance growing with bacterial contamination? Be careful of what you see. These resolutions may seem comforting, but it is a false comfort. Take the 200 pH as the reading and leave the bouncing numbers off.

**Pulse-Current-Injection**

We believe that the best way to verify any claim is to use multiple methods to test the claim that result in the same measurement. Another method of testing for ESL, ESR and effective capacitance is by using a current pulse injection system. A pulse can be verified with no capacitor by terminating the pulse generator with its characteristic impedance. We use a pulse generator from HP (HP-2148) for transitions down to 10 nS, and a model 200 Pulse generator from Pico Pulse Labs with a transition time less than 500 pS. The current pulse transitions from zero current to the output level of the pulse generator and will hold, at that level, for the duration of the pulse.

By injecting the current pulse into the device, the resultant voltage across the device can be analyzed to determine the capacitive, resistive, and inductive elements of the device.

In a perfect resistor (Figure 13 upper left), the resultant voltage pulse would be similar in shape to the current pulse. It should mimic the transition current from zero to the constant current mode, and then hold at a specific voltage during the constant current mode.

For a perfect capacitor (no ESR and no ESL as in Figure 13, upper right), the voltage will show an exponential growth during the current pulse transition time (tr), and then should reveal a constant dv/dt during the constant current phase (I_{const}). The calculation for the exponentially rising voltage for any time (t_i) during the transitions is as follows:

\[
V_{c(t)} = V_{const} \times \frac{t_i}{2} \quad (0 \leq t_i \leq t_r)
\]

Equation 1

For a pure inductor (Figure 13, bottom center), the voltage will be increasing (V=L*di/dt) as the current is in transition and should drop to zero once the current reaches its constant mode. What disturbs this effect is that the voltage cannot immediately drop to zero as the combination of inductor, capacitor, and resistor (including source and load resistors) creates a loop that will allow this voltage to ring down to zero.
The cumulative pulse response to the capacitors is a combination of all of the pure elements as shown in Figure 14. In this analysis, the capacitance is first derived from the constant dv/dt slope, after the ringing effect has died down. At the time values t1 and t2, the voltages v1 and v2 are extracted, and the capacitance is calculated using these values and the known constant current. Once this capacitance is derived, the voltage at the transition time can be calculated using Equation 1 with ti set to be equal to the transition time (tr). The difference between this voltage and the extrapolated voltage based on the dv/dt extension from the points (t1,v1) and (t2,v2), will define the resistive offset voltage.

\[
C = \frac{I_{\text{const}} \times (t_2 - t_1)}{(v_2 - v_1)}
\]

For electrolytic capacitors, the capacitance will appear to have an RC-Ladder structure. In frequency scans, the capacitance begin to decay after a specific frequency is exceeded. Lowering the ESR in these
components does shift the frequency where this decay begins at a higher frequency range, but it still occurs. With some of the low ESR conductive polymer devices, this decay has been moved to frequencies above the self-resonant frequency. With this current pulse injection method, the constant dv/dt slope appears to be not constant. The slope is steep at the beginning (low capacitance) and the slope decays until it appears constant. Once this slope appears constant, the nameplate voltage is normally derived. Figure 15 is the image captured from a conductive polymer capacitor with very low ESR. The changing dv/dt slope after the ringing has decayed is very minimal – almost imperceptible. The equipment required to make these measurements is definitely not as expensive as network analyzers with high precision and wide frequency range. The storage oscilloscope for capturing these voltage responses may already be sitting on a bench in you facility.

![Figure 15. Cumulative voltage response from conductive polymer capacitor to current pulse.](image)

**Summation**

The goals of reducing the parasitic elements in capacitors are constantly being pursued and constantly moving to ever decreasing levels. Within the capacitor manufacturing community, there is an ongoing clash between engineering fact and marketing one-upmanship. Can the user achieve ESLs that match the claims of the component manufacturer? Because we tend to measure the component by itself, a match with in circuit response is unlikely; but it should not be vastly different. We do not incorporate the lead traces or the vias required to mount these components in a vast variation of circuit designs. Be careful of the claims of two manufacturers making the same device with vastly different claims on performance. The name on the shipping label cannot create these differences in like components. The best analysis of what a component does in a specific circuit is the response of those components in that circuit.

**Bibliography**