Measuring the Power Dissipation Capability of High-Voltage, Low-Capacitance Ceramic Chip Capacitors

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Abstract

This paper describes a successful strategy for measuring the power dissipated by high-voltage, low-capacitance ceramic chip capacitors at frequencies typical of switch-mode power supplies. For these devices, the simpler techniques employed to measure the power dissipation of high-capacitance tantalum and aluminum devices prove inadequate, and a more fundamental approach is required.

The various measurement complications presented by high-voltage, low-capacitance ceramic chip capacitors are explored. Test circuitry is described that facilitates the necessary measurements. Representative raw and processed test data are presented to fully demonstrate the technique. Finally, general observations are made about the electrical and thermal performance of this class of ceramic chip capacitors.

Introduction

Capacitors are frequently used in circuits that expose them to significant ripple voltage and current. Power is dissipated in the resistive component of the capacitor's impedance by the ripple current, and this power dissipates heat which causes the capacitor's temperature to rise. Both manufacturers and users need to know how much power is dissipated at a given level of ripple current or voltage and how much temperature rise can be expected per watt of dissipated power.

For high-capacitance valve-metal capacitors such as tantalum, niobium, and aluminum capacitors, the methodology for measuring these characteristics is fairly straightforward.[1] First, the equivalent series resistance (ESR) of the target device is measured over a suitable temperature range at low signal levels. Ripple current is then applied at several, much higher test signal levels and the device temperature rise is measured with the device mounted in a standard configuration.

Power dissipation is calculated as $P=I^2*ESR$ at each ripple level, and temperature rise versus power dissipation curves or temperature rise versus ripple current curves are created. Appropriate limits are established upon inspection of these performance curves. The process is simplified by the fact that the device's ESR is not significantly affected by the test signal level other than a small secondary effect from the device's temperature rise.

It is much more difficult to characterize the power dissipation performance of high-voltage, low-capacitance, medium-K (K=1000-4000) ceramic chip capacitors. The ESR of these devices is not only very sensitive to temperature, but is also strongly sensitive to the magnitude of the applied voltage (both the AC and DC components).[2]

Compounding the difficulty, conventional automatic impedance measurement instruments rarely generate test signal levels much higher than about 1.0 Vrms. This limited signal strength makes it difficult to characterize the AC voltage sensitivity of ESR at levels high enough to generate significant self-heating. Thus the

straightforward methodology described for high-capacitance valve-metal capacitors does not apply to the characterization of high-voltage, low-capacitance ceramic capacitors.

Imperfections of Ceramic Capacitors

It is not uncommon for the ESR and capacitance of valve-metal capacitors (tantalum, niobium, and aluminum) to be relatively stable in the frequency range typical of switch-mode power supplies (40 kHz to 2 MHz). In this frequency range, the ESR and capacitance of valve-metal capacitors responds primarily to device temperature. There is some sensitivity to frequency and voltage, but this sensitivity is usually small enough to ignore. For almost all surface-mount valve-metal capacitors used in this frequency range, it is common for ESR to remain within a range of roughly 1.5:1, and for capacitance to remain within a range of roughly 1.2:1, when the capacitor is exposed to normal operating conditions. Unfortunately, this is distinctly not the case for medium-K ceramic chip capacitors.

As was previously mentioned, the ESR of medium-K ceramic capacitors is not very stable and is sensitive to various factors. Like valve-metal capacitors, medium-K ceramic capacitors are sensitive to temperature. But there is a distinct difference in the level of sensitivity. The ESR of medium-K ceramic capacitors can change by a ratio as large as 10:1 as temperature changes from 25^{o}C to 125^{o}C. The ESR typically falls with increasing temperature as the dipoles in the dielectric polarize with decreased loss at higher temperatures.

The ESR of medium-K ceramic capacitors is also sensitive to the applied AC electric field (AC voltage). Generally, the ESR increases with moderate AC voltage application as the dipoles in the dielectric are forced to polarize in a less linear fashion as the AC voltage increases. Also, mechanical losses are incurred as piezo-electric responses are driven by the applied AC electric field. However, as voltage is further increased, and significant self-heating begins to occur, the ESR increase is eventually overshadowed by temperature-driven ESR reduction.

The ESR of medium-K ceramic capacitors is also affected by DC electric fields. The response is similar in nature to the AC response, but has smaller magnitude.

Not only is ESR affected by temperature and voltage, but also the capacitance (and, thus, the reactance and impedance) of the capacitor is significantly affected. Capacitance change can easily exceed a ratio of 2:1 with changes in temperature and voltage. This complicates the measurement of dissipated power because the ratio of applied ripple voltage to resulting ripple current is not constant, and for a fixed application of ripple voltage the resulting ripple current cannot be determined until the capacitor reaches thermal equilibrium.

Moreover, significant voltage-driven changes in ESR and capacitance can occur within a single cycle of the applied AC voltage waveform. The result is a non-linear current response to the instantaneous applied voltage. Specifically, non-sinusoidal current is generated by application of high-level sinusoidal voltages. Distortion of the current waveform makes it all but impossible to accurately identify the phase angle of the current waveform with respect to the voltage waveform by visual inspection, the basis for one traditional method of calculating ESR ($ESR=[V/I]*\cos\Theta$). This is not surprising since the concept of phase angle strictly applies only to purely sinusoidal waveforms.

In summary, the impedance and ESR of medium-K ceramic capacitors change dramatically with temperature and voltage. It is difficult to measure capacitance and ESR at typical operating voltages because these voltages exceed the signal levels available from common impedance analyzers. Also, because the voltage-current response is non-linear at high signal levels, ESR and power dissipation cannot be accurately determined from simple phase-difference measurements between the voltage and current waveforms. Faced with these complications, just how does one measure the power dissipation of medium-K ceramic capacitors at high voltage levels?

A Fundamental Approach

One approach to this problem is to configure a high-power impedance analyzer so that the electrical state of the capacitor can be measured, in situ, while it is exposed to the desired high test signal levels and its temperature rise is measured. With knowledge of the root-mean-square (rms) current and the capacitor's ESR at the frequency of interest, the dissipated power can then be calculated. In principle this can be accomplished by amplifying the oscillator drive signal from a conventional impedance analyzer and then attenuating the response signals from the device under test before sensing them with the analyzer.

Unfortunately, practical application of this concept has proven difficult. Several problems remain to be solved to achieve success. Among them are (1) achieving adequate noise attenuation and ground isolation in the high-power amplifier to allow stable performance of the control loops of the impedance analyzer, (2) attenuating the resulting voltage and current to levels compatible with the input sense circuitry of the analyzer, and (3) controlling phase shifts in the amplifier and attenuators so that the analyzer's auto-balance circuitry operates correctly and measurement errors remain within the range that can be corrected with the analyzer's error compensation routines.

The successful solution that is described in this paper is based on the same "high-power impedance analyzer" concept described above, in that the capacitor's electrical state is completely characterized while the capacitor is exposed to the desired high test signal levels and the capacitor's temperature rise is measured. But to circumvent the interface problems between a "store-bought" impedance analyzer, the power amplifier, and the voltage and current attenuators, a high-performance digital oscilloscope and a stable signal generator are substituted for the impedance analyzer.

In this measurement method, true rms power is calculated directly from the measured voltage and current as the time-weighted integral (constant average value) of the product of their waveforms. Once the true average dissipated power is calculated from the measured voltage and current at the frequency of interest, all other electrical parameters can be calculated from this information. The circuit and calculations employed are discussed in the next section.

The keys to the success of this technique are (1) accurate high-voltage measurement, (2) accurate current measurement, and (3) precise and stable time (phase) delay between the voltage and current measurement circuits. The steps taken to maximize each of these favorable characteristics are also described in the next section.

A few comments on the fundamental nature of these measurements are in order. The non-linear relationship between the instantaneous voltage and current in medium-K ceramic capacitors results in non-sinusoidal current from sinusoidal excitation voltage. This situation implies time-varying impedance of the capacitor over each cycle of the exciting voltage. Traditional circuit theory recognizes capacitors which have only constant impedance at a chosen frequency, and which produce sinusoidal current when driven by sinusoidal voltage.

So at the moment that this constant-impedance condition is not met, it is no longer possible to know the "exact" impedance, ESR, phase angle, or capacitance of such a device. The best that is possible is to determine the "effective" values of these parameters over the period of the exciting waveform.

These effective impedance values represent the performance of a similarly valued linear capacitor that is excited with the same rms AC voltage and produces the same rms AC current and dissipated power. This "effective impedance" approximation is not really any different from that performed when measuring the rms values of AC voltage, current, and power. For these parameters, their instantaneous values are constantly changing with time during each cycle of the exciting voltage, but their rms or effective values can be constant from cycle to cycle.

The method of assigning effective impedance values to non-linear capacitors can lead to measurement discrepancies between measurement systems that otherwise produce consistent results when measuring linear capacitors. As long as effective impedance values are calculated from rms values of voltage and current, there should be no

discrepancy. But if the "rms" measurements of voltage and current in the measurement system are actually *average* values of voltage and current that are corrected by a factor that converts the average value of a sinusoidal signal to its rms value (e.g., the $0.707V_{pk}/0.637V_{pk}$ correction factor of common averaging voltmeters), then there will be an inherent error in the reported effective impedance values that grows with the percent distortion in the voltage and current waveforms (the "crest" factor of the waveforms).

The Measurement Circuit

The measurement circuit employed to collect the data presented in this paper appears in Figure 1. A stable function generator (Agilent 33120A) drives an ENI EGR-1600 power generator which is coupled to the device under test by a hand-wound ferrite toroidal matching transformer.

Current is measured by an Agilent Infiniium 1GHz, 4MSa/s digital oscilloscope as the voltage drop across a precision, low-inductance 0.1Ω, 1% metal-film sense resistor. This resistor is directly in series with only the device under test. The approximate probe attenuation/conversion ratio from measured voltage to displayed current is 10:1 (the actual calibrated ratio was 10.11:1 at 100 kHz).

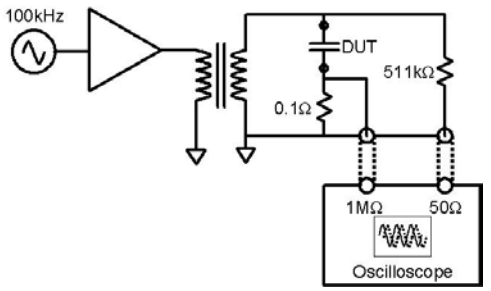

Figure 1. Circuit Used to Measure Power Dissipation and Impedance Characteristics of High-Voltage, Low-Capacitance Ceramic Capacitors.

Voltage is measured across both the device under test and the 0.1Ω resistor with a hand-built voltage divider constructed of ten ¼ watt, 51.1k Ω, 1% metal-film resistors connected in series with the 50 Ω input of an oscilloscope channel via a 50 Ω coaxial cable. Error from the voltage drop across the 0.1Ω resistor is very small for the range of measured impedances expected during this testing (typical Zdut > 100Ω), and it is ignored. The approximate probe attenuation ratio is 10000:1 (actual calibrated ratio was 10210:1 at 100 kHz).

These resistance values were chosen to best balance the competing needs for: (1) low power dissipation in the voltage divider at high voltages, (2) low noise sensitivity, and (3) significant attenuation to limit the voltage seen by the oscilloscope with high voltage applied to the device under test (DUT). The 511kΩ voltage divider resistor was constructed of 10 series-connected metal film resistors to minimize the voltage across each resistor at high excitation voltages. This physical construction minimizes the error caused by the voltage coefficient of resistance of these resistors.

Figure 2. General Configuration of Test Instrumentation.

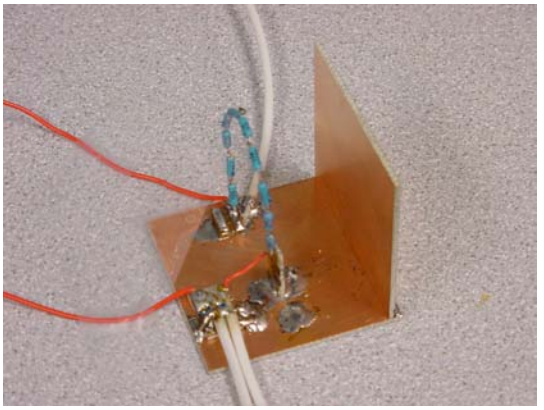

Figure 3. Close-up of the Current and Voltage Probe Fixture.

The general layout of the test system appears in the photograph of Figure 2. A closer view of the current and voltage probe fixture appears in the photograph of Figure 3. The cable exiting the top of the picture leads to the matching transformer and amplifier while the cables exiting the bottom of the picture lead to the oscilloscope. The wires exiting from the left of the picture lead to the device under test.

The current and voltage probe attenuation ratios were set to provide amplitude agreement at 100 kHz with an HP 34401A digital voltmeter while using an HP 16384A 1000pF standard air capacitor as the DUT and 300 Vrms for excitation. So adjusted, the test circuit measured the impedance of the standard capacitor to within 0.5% of its calibrated value when the waveforms were sampled at approximately 160 MSa/s and averaged 16 times.

One final critical adjustment was made to the current measurement channel while the standard air capacitor was connected and excited with 300 Vrms. A parameter called "probe skew" was adjusted to compensate for unequal time delay between the current measurement circuit and the voltage measurement circuit. Proper adjustment was achieved when the phase difference between the voltage and current was exactly 90.00 degrees – the proper phase difference for this near-ideal air-dielectric capacitor. The final adjustment was -74.5ns which is equivalent to a phase correction of -2.682 degrees at 100 kHz.

During the circuit development process it was found that the "probe skew" adjustment was sensitive to the proximity of the operator's body to the voltage divider resistor chain. An electrostatic shield plate was installed on the probe circuit board to isolate the voltage divider from human capacitance while still allowing adequate airflow to keep the resistors cool.

Upon reflection, it probably makes more sense to apply the "probe skew" adjustment to the voltage measurement channel rather than to the current measurement channel. This is because the relatively higher impedance of the voltage divider circuit is more sensitive to parasitic capacitance and contributes more phase error than does the very low impedance current measurement circuit. However the only practical difference regarding which measurement channel is adjusted is the sign of the adjustment.

Measurements

In this section, one complete measurement of an 0805, 820 pF, 1000V ceramic chip capacitor is documented to demonstrate the details of the measurement technique. The excitation voltage was set to 100 Vrms for this measurement.

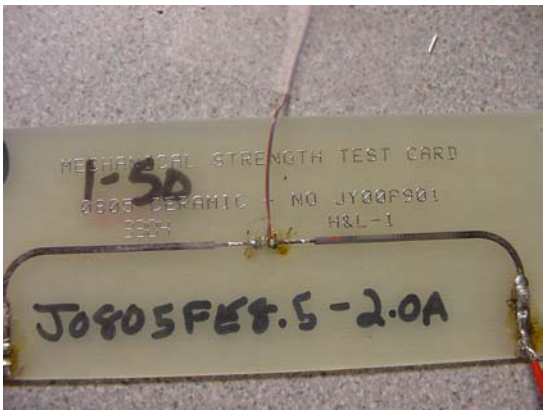

Figure 4. Test Card with 0805, 820pF, 1000V Ceramic Chip Capacitor Mounted Thereon and a Small-Gage Thermocouple Attached to the Capacitor.

A picture of the test card and the device under test appears in Figure 4. While not necessarily a good example of optimized thermal management,

temperature rise versus power dissipation data measured with this mounting configuration should prove to be very conservative. That is, customers will certainly see better thermal performance if they take active measures to improve heat extraction from the capacitor. Such measures could include the use of broader and thicker circuit traces or the addition of forced-air cooling.

Wires soldered to the test card lead to the probe fixture. The thermocouple is attached to a Wahl model C-65 thermocouple calibration standard which is used for surface temperature measurements.

A magnified view of the ceramic chip and the attachment of a small-gage thermocouple to the surface of the capacitor appear in Figure 5. The wire size of the thermocouple is #36 (0.005 inch diameter) and the thermocouple is type-T. Five mil wire is about as small a wire size as is practical to work with without specialized equipment.

The small wire size was chosen to allow electrical isolation between the thermocouple and the capacitor's metallic terminations, and to minimize thermal loading caused by the presence of thethermocouple on the chip's surface. The thermocouple is attached to the chip with cyanoacrylate adhesive ("super glue").

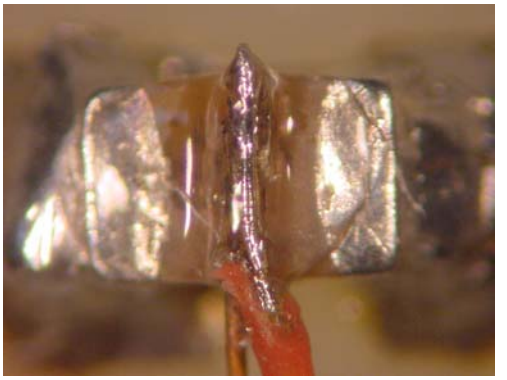

Figure 5. Magnified View of a Ceramic Chip Capacitor and a Small-Gage Thermocouple Attached to the Capacitor's Surface.

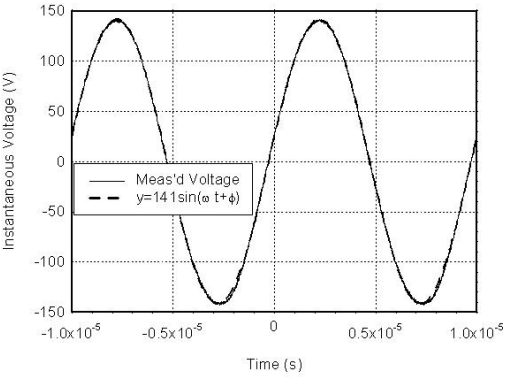

Figure 6. Measured and Ideal Voltage Waveforms for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited with a 100Vrms Test Signal at 100kHz.

Two cycles of the voltage and current waveforms resulting from the 100 Vrms excitation appear in Figures 6 and 7, respectively. Each figure contains the measured waveform and an idealized sinusoidal waveform. At 100 Vrms, the measured voltage waveform appears to be essentially sinusoidal, but the current waveform demonstrates visible distortion in the general neighborhood of its positive-going zero crossings. This distortion becomes progressively more evident as the excitation voltage is increased from 100 Vrms to 350 Vrms.

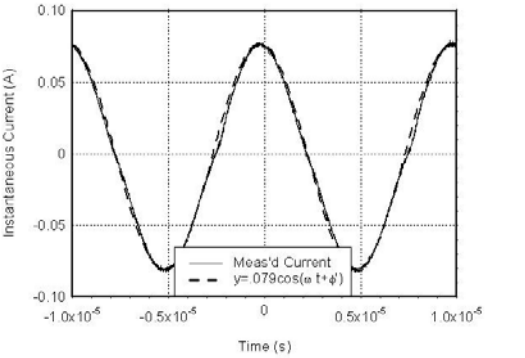

Figure 7. Measured and Ideal Current Waveforms for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited with a 100Vrms Test Signal at 100kHz.

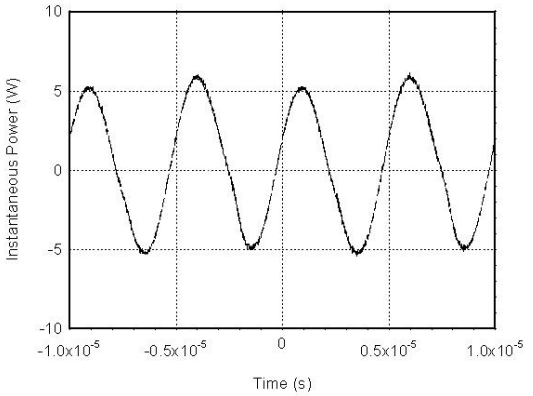

Figure 8. Calculated Instantaneous Power during Charging and Discharging of an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited with a 100Vrms Test Signal at 100kHz.

The next step in the measurement process is to calculate the product of the voltage and current waveforms. This product provides a time record of the instantaneous power involved in charging and discharging the capacitor. The calculation is performed automatically by a math function of the oscilloscope. The waveform appears in Figure 8.

If one observes the waveform in Figure 8, he sees that approximately half of the time there is positive power consumed while the capacitor is charged. During the balance of the time, the capacitor is discharging into the amplifier and the instantaneous power is negative. On average, however, there is a little more positive power than negative power. This imbalance represents the power consumed by the ESR of the capacitor. This power is lost to the environment in the form of heat and causes the capacitor's temperature to rise.

It is difficult to quantify the average dissipated power directly from the waveform in Figure 8. So this waveform is integrated to find the instantaneous energy captured and returned by the capacitor over time. Deriving the average dissipated power from the integrated waveform is straightforward.

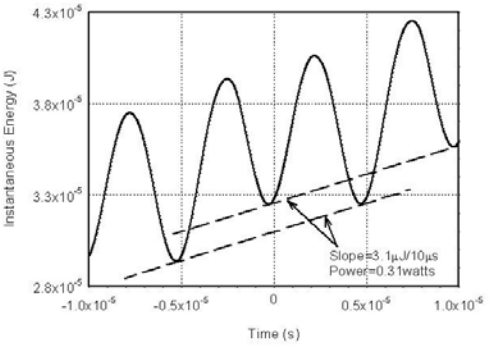

Figure 9. *Calculated Instantaneous Energy during Charging and Discharging of an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited with a 100Vrms Test Signal at 100kHz.*

The integration calculation mentioned above is also performed automatically by a math function of the oscilloscope. The integral of the instantaneous power waveform of Figure 8 appears as a plot of instantaneous energy in Figure 9. It is clear that over time the capacitor steadily consumes more energy than it returns.

The average slope of the energy-time plot of Figure 9 yields the average power dissipated by the capacitor. As noted on the graph, approximately 3.1 μJ of energy is consumed in exactly 10 μs, the period of a 100 kHz waveform. Since power is energy consumed per unit time, the average power dissipation is approximately 3.1μJ/10μs=0.31W with 100Vrms applied.

The temperature rise above ambient was measured and found to be 37.9°C. This yields a thermal resistance of approximately 120°C/W for this capacitor in its specific mounting configuration.

The marker functions of the oscilloscope are set to report the instantaneous energy at two suitable points on the instantaneous energy waveform and also to report the time difference between these points. The average dissipated power is calculated by dividing the difference in energy (ΔU) by the difference in time (Δt).

A picture of the oscilloscope screen which includes the voltage, current, instantaneous power, instantaneous energy, and the markers used to calculate the slope of the energy waveform to find average dissipated power appears in Figure 10. Numerical data are reported at the bottom of the oscilloscope screen for both the rms voltage and rms current. When the "Markers" tab is clicked, the delta-energy and delta-time data are reported.

Figure 10. Voltage, Current, Power, and Energy Waveforms and Energy Consumption Markers as Displayed on the Oscilloscope Screen.

Impedance Calculations

The measurement process described above yields rms voltage, rms current, dissipated power, and temperature rise. Thus the primary objective of this paper has been achieved. That is, an accurate technique has been described to characterize the power dissipation capability of high-voltage, low-capacitance, medium-K ceramic chip capacitors.

Once these data are collected at different levels of excitation, plots of temperature rise versus power dissipation and temperature rise versus ripple current or voltage level can be generated for various mounting configurations. But much more information can be extracted from the data.

Specifically, it is possible to completely describe the impedance of the test capacitor from the voltage, current, and power dissipation data. Thus the described measurement system is actually a high-power impedance analyzer. The formulas needed to convert the measured data to the impedance characteristics of interest are given below.

V V_{rms}	I mA_{rms}	ΔU µJ	Δt_U µs	P W	Z Ω	ESR Ω	X_c Ω	C pF	DF %	T_{meas} °C	T_{amb} °C	ΔT °C	R_{th} °C/W
20.00	10.26	2.10	190	0.011	1949	105	1946	818	5.4	27.6	26.1	1.5	136
35.00	18.48	7.90	190	0.042	1894	122	1890	842	6.5	30.9	26.1	4.8	115
50.00	27.15	19.3	190	0.102	1841	138	1836	867	7.5	38.4	26.0	12.4	122
60.00	33.17	30.7	190	0.162	1809	147	1802	883	8.2	44.8	26.0	18.8	116
70.00	38.92	40.0	190	0.211	1799	139	1793	888	7.8	51.2	26.1	25.1	119
80.00	44.27	47.9	190	0.252	1807	129	1802	883	7.2	57.1	26.0	31.1	123
100.0	54.22	59.3	190	0.312	1844	106	1841	864	5.8	64.0	26.1	37.9	121
130.0	67.75	69.3	190	0.365	1919	79.5	1917	830	4.2	69.6	26.1	43.5	119
160.0	79.99	73.6	190	0.388	2000	60.6	1999	796	3.0	73.1	26.1	47.0	121
200.0	94.76	77.2	190	0.407	2110	45.3	2110	754	2.2	75.6	26.2	49.4	121
250.0	110.7	82.2	190	0.433	2259	35.4	2258	705	1.6	78.2	26.3	51.9	120
300.0	123.2	87.2	190	0.459	2435	30.3	2435	654	1.2	81.7	26.4	55.3	120
350.0	130.9	96.5	190	0.508	2674	29.7	2674	595	1.1	87.5	26.5	61.0	120

Table 1. Measured and Calculated Data for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited at 100 kHz (measured data are shaded, calculated data are un-shaded).

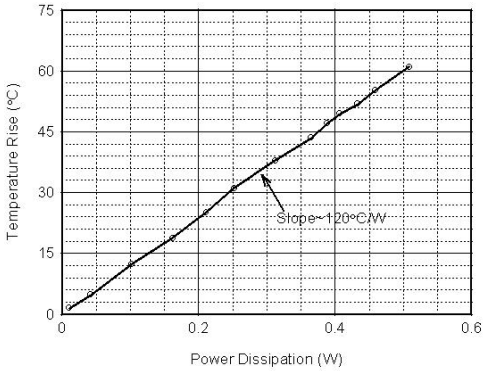

Figure 11. Temperature Rise versus Power Dissipation Data for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited at 100kHz.

First, the impedance of the DUT can be calculated by simple division: Z=Vrms/Irms. Now, since the average dissipated power is known, one can calculate the ESR of the DUT with this formula: $ESR=P/I^2rms$.

With ESR known, the capacitive reactance can be found: $Xc=Sqrt(Z^2-ESR^2)$. Given the capacitive measured data is that the slope of the curve is fairly constant. In reality, more error was created by unstable air currents (from the plant air conditioning system) than was caused by the measurement system.

Another plot of interest is temperature rise versus ripple current. These data appear in Figure 12. The irregular slope of this curve implies that the ESR of the capacitor is not constant as the ripple current rises.

The ESR versus rms voltage data of Table 1 appear in Figure 13. As described earlier in the paper, ESR initially increases with increasing AC voltage. But, eventually self heating forces a dramatic decrease in ESR. The conflict between these two processes is evident in the graph. Also noteworthy is that the ESR changes over almost a 5:1 range as the surface temperature rises from 44.7°C to 81.7°C which is only a 37°C temperature rise.

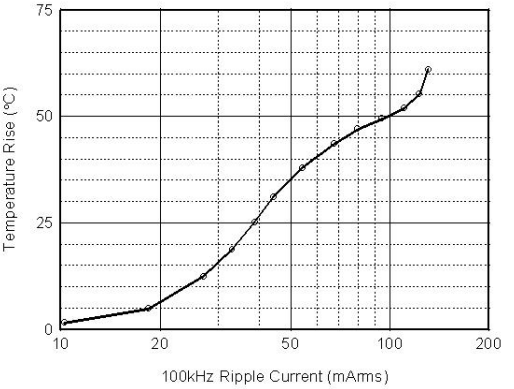

Figure 12. Temperature Rise versus Ripple Current Data for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited at 100kHz.

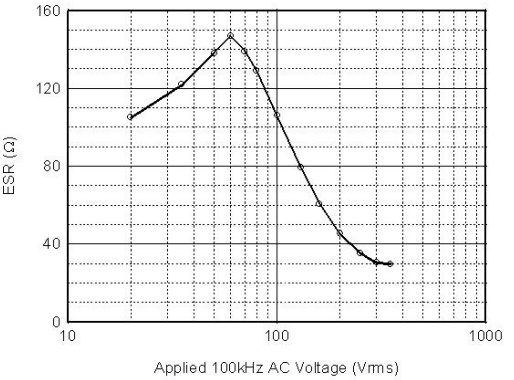

Figure 13. ESR versus rms AC Voltage for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited at 100kHz.

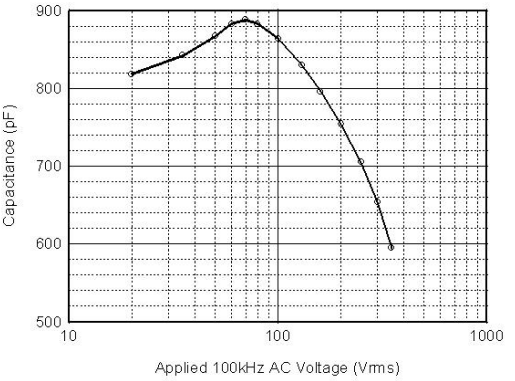

Figure 14. Capacitance versus rms AC Voltage for an 0805, 820pF, 1000V Ceramic Chip Capacitor Excited at 100kHz.

One observes a similar, but not quite as dramatic effect in the capacitance versus rms voltage data of Figure 14. The capacitance initially rises as the voltage is increased, but then falls as the capacitor's temperature rises.

Summary and Conclusion

Low-capacitance, high-voltage, medium-K ceramic chip capacitors present many challenges as one attempts to accurately characterize their power dissipation characteristics at high signal levels. The non-ideal impedance characteristics of these capacitors thwart traditional approaches to such measurements. One would like to use commercially available impedance analyzers to both excite and measure the capacitors at high signal levels, but these analyzers are not capable of the voltage or power levels needed to create significant device temperature rise. Also, many analyzers do not respond gracefully to the waveform distortion that can occur in these capacitors at high signal levels.

A measurement technique is presented in this paper that circumvents these obstacles. Energy consumption by the capacitor is measured directly as the time-weighted integral of the instantaneous voltage and current as observed with a digital oscilloscope. In order for these data to be accurate, care is taken to probe the voltage and current accurately, and to precisely establish the time delay (phase shift) between the voltage and current probes and their respective measurement circuitry in the oscilloscope.

Having achieved the primary objective of the project (power dissipation characterization), it was discovered that much more information is present in the measured data than was first recognized. That is, the measured data are sufficient to provide complete impedance information about the device under test at high test signal levels. This bonus information provides the ability to directly report the effects of high ripple voltage and ripple current on the ESR and capacitance of the tested device. These data visually demonstrate the various imperfections of these ceramic capacitors that complicate more traditional measurement approaches.

In conclusion, while these capacitors are very useful to circuit designers, they present significant challenges to the conscientious measurement engineer. But as is true in many aspects of engineering, when simple approaches fail, get back to the basics. In this case, direct measurement of the dissipated power via time-weighted integration of the product of the instantaneous voltage and current is the key to success. There is no more fundamental way to measure average electric power in AC circuits.

References

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