

HIGHLY ACCELERATED LIFETESTING (HALT) OF KEMET BASE-METAL-ELECTRODE (BME) CERAMIC CHIP CAPACITORS

Jonathan L. Paulsen
Erik K. Reed
KEMET Electronics Corporation
PO Box 5928 Greenville, SC 29606
864-963-6300 Phone
864-963-6322 Fax

ABSTRACT

The ever-growing price of precious metals has promoted the widespread use of nickel and copper in the internal electrodes and end terminations of multilayer ceramic capacitors (MLCCs). While these base metal electrode (BME) capacitors are less expensive than capacitors made with palladium and silver/palladium, their unique production process produces an identifiable wear-out mechanism. Highly accelerated lifetesting is used to evaluate the reliability of BME MLCCs within reasonable timeframes by using high electric field stress and high temperature. The results of this testing are fit to a well known reliability model and then the model is used to predict device reliability under maximum rated conditions for these capacitors. Median life, t_{50} , is found to be in excess of 1000 years at maximum rated conditions.

INTRODUCTION

As the market price of many multilayer ceramic capacitors (MLCCs) fell to pennies per part, the use of palladium in the internal electrodes of these devices became increasingly unprofitable. Indeed, the cost of palladium has skyrocketed from around \$150 per troy ounce in the mid-nineties to over \$1000 per troy ounce today. The use of silver/palladium alloy, rather than pure palladium, is one way to lower costs. Another solution is replacing these precious metals with less costly base metals.

The production of capacitors with electrodes made of base metals such as nickel or copper requires a reducing atmosphere to protect these metals from oxidation during firing. "Oxygen vacancies" left behind in the dielectric by this process lower the device's insulation resistance and degrade its reliability.

To reduce the number of oxygen vacancies, dopants are added to the dielectric material and a reoxidation

process is performed after firing. These steps restore the quality of the dielectric significantly, but not completely. Oxygen vacancies remain, and these vacancies are thought to migrate through the dielectric while the capacitor is energized. This migration eventually leads to device failure.

Due to knowledge of this "wear-out" mechanism, customers have expressed concern over the reliability of BME capacitors. The purpose of this present work is to use highly accelerated life testing (HALT) to assess the reliability of BME capacitors when used at or below their rated conditions. HALT testing provides a means for one to characterize the reliability of BME capacitors under rather severe conditions, and then extrapolate the reliability of these devices under more typical application conditions using the data collected using the highly accelerated testing.

The theoretical underpinnings of the HALT methodology are briefly explained, the time-to-failure data under various test conditions are presented, and projections of expected reliability are made. Strengths and weaknesses of the method are identified, including potential sources of error.

HALT TESTING

Acceleration in time of multilayer ceramic chip capacitor lifetest failures as a function of voltage and temperature is commonly modeled by the following empirical equation suggested by Prokopowicz and Vaskas¹.

$$A = \frac{t_1}{t_2} = \left(\frac{V_2}{V_1} \right)^n \exp \left[\frac{E_a}{k} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right]$$

The variable A has been added to Prokopowicz and Vaskas' equation to more explicitly highlight the link between *accelerated* time and the variables voltage and temperature. A is the ratio of two times-to-failure, or the *acceleration factor* relating time-to-failure under one set of conditions (of voltage and temperature) to time-to-failure under a second set of conditions.

Since it is not possible to experimentally determine more than one time-to-failure per device when testing ceramic chip capacitors, the times-to-failure t_1 and t_2 are commonly taken as the times t_{50} , or *median life*, when half of the devices in a sample population have failed. The statistic t_{50} should not be confused with the statistic *mean time to failure* (MTTF) which is most properly used to describe devices whose lifetimes have an exponential distribution and which display a constant failure rate.²

It is common for ceramic capacitor times-to-failure to fit a log-normal distribution. However, occasionally a researcher will choose to fit times-to-failure to a Weibull distribution. In this case it is more likely that he will choose the statistic $t_{63.2}$, the *characteristic life* of the samples, for the variables t_1 and t_2 . Both statistics, t_{50} and $t_{63.2}$, yield similar results from the acceleration equation. In this study, times-to-failure are fit to a log-normal distribution and the median life, t_{50} , is chosen as the time statistic.

The stress variables are voltage and absolute temperature. The equation implies that these stresses are independent of each other, but experimental data indicate some interaction between the two stress variables.

The acceleration of time-to-failure due to changes in voltage is a power function of the ratio of the two voltages. Historically, the exponent n was found to be in the neighborhood of 3.0, but tests of new, higher-K dielectrics that are fabricated with smaller absolute sheet thickness have yielded voltage-ratio exponents exceeding twice this value.

The acceleration of time-to-failure due to changes in absolute temperature is modeled as an Arrhenius equation. The critical factor in Arrhenius equations is

the *activation energy*, E_a , which is assumed to have constant value and is generally experimentally derived. The validity of the assumption of constant activation energy over wide ranges of temperature is suspect, but remarkably consistent values have been observed over moderate ranges of temperature.

The constant k is Boltzmann's constant whose value is approximately $8.6E-5$ eV/K. Absolute temperature in kelvins is approximately the temperature in Celcius degrees plus 273.

The *methodology* of HALT testing is as follows: (1) multiple failure distributions are generated at various combinations of voltage and temperature (generally quite harsh), (2) the degree of acceleration caused by changes in voltage and absolute temperature (observed separately) is quantified as the ratio of times t_{50} , and (3) values of n and E_a are determined so as to best fit the acceleration equation to the experimental data. The *objective* of HALT testing is to predict the median life of devices under normal, non-accelerated operating conditions by applying the acceleration equation in combination with the derived values of n and E_a , and the known median life under accelerated conditions.

The expected lifetimes of electronic components are very long, perhaps decades, centuries, or longer. Thus it is necessary to collect time-to-failure data under highly accelerated test conditions, use this data to estimate n and E_a , and then use the acceleration equation to predict median life under normal, less stressful conditions. Of course, there is always danger associated with extrapolating performance outside the space of the original experimental data. However, there are few alternatives available to effectively quantify the expected reliability of such reliable devices in a practical timeframe.

Efforts have been made to present the data of this study in a format that allows the reader to judge the degree of uncertainty introduced by extrapolating results outside of the experimental space. Evidence of interaction between voltage stress and temperature stress exists, but the behavior of the devices within the experimental space is such that extrapolation outside of this space to more normal use conditions appears to be reasonable. Also, the predicted reliability of the devices under normal operating conditions is sufficiently high that prediction errors approaching an order of magnitude are not likely to cause alarm.

ANALYSIS OF KEMET BME TIME-TO-FAILURE DATA

Figure 1 is a crowded graph that contains all of the time-to-failure data collected from a batch of KEMET BME 0.1uF, 50V ceramic chip capacitors. The same data will presently be viewed in subsets, but one can make important observations by viewing all of the data at one time.

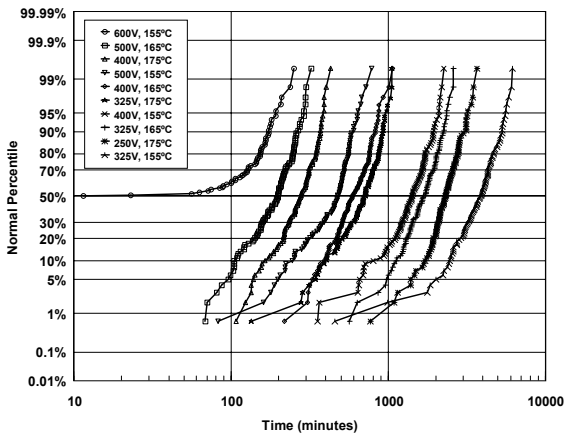


Fig. 1. Lognormal Plot of Failure Percentile versus Time-to-Failure for KEMET BME.

The test conditions included three temperatures (155°C, 165°C, and 175°C) and five voltages (250V, 325V, 400V, 500V, and 600V). Median life under the various test conditions ranged over almost two orders of magnitude (115 minutes to 3649 minutes).

Three failure mechanisms are of interest when lifetesting MLCCs: Infant mortals, freaks, and wearout failures. Infant mortals contain major construction defects and never function properly. Freak failures have minor construction defects that will eventually cause failure, but perhaps years after initial usage. Wearout failures, the focus of this experiment, only occur after the dielectric within the capacitor changes due to applied electric field stress. HALT testing is a good method to diagnose all three of these mechanisms. On a time-to-failure graph, each failure mechanism will appear as a subpopulation requiring a different “best fit” line. Some of the early failures on the graphs shown may be attributable to freak failures, their presence causing a slight curve at the bottom of the distribution. Despite justified interest in these failures, they have been ignored in this discussion of wearout, and not used in the statistical calculations.

The relatively straight lines on the graph suggest that the majority of the failures were caused by one failure mechanism. Given the severity of HALT testing, it is important to note that no new failure mechanisms were introduced.

The data collected at 600V are shaped differently from the other failure distributions because of limitations of the test system. The system ramps up the test voltage over a significant period of time before it starts collecting time-to-failure data. Consequently, significant stress is applied to the capacitors prior to the start of data collection, which can cause the reported early-time failures to be excessively large. However, at later test times, the relatively small time-error introduced at the start of the test ceases to influence the later failure times after roughly 120 minutes, and a reasonable estimate of t_{50} can be extrapolated from the later-time failures.

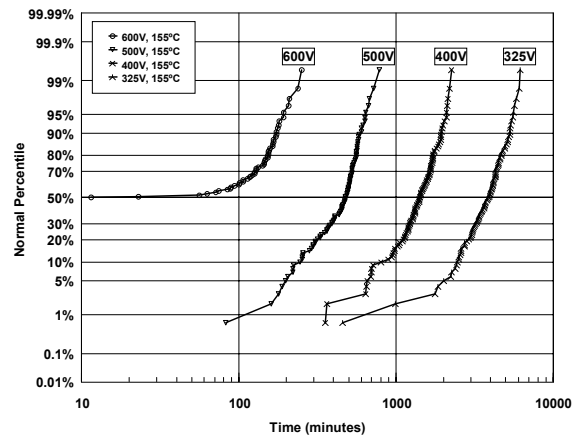


Fig. 2. Lognormal Plot of Failure Percentile versus Time-to-Failure at 325V, 400V, 500V, and 600V for tests done at 155°C.

Data collected at 155°C and four voltages appear in Figure 2. It is clear that the failure distributions are similar (excluding the anomalous early-time failures in the 600V curve) and that the spacing is reasonably uniform as the voltage is changed from 500V to 400V to 325V (similar percentage shifts in voltage). It seems reasonable to project that further decreases in voltage would produce failure distributions whose only difference would be longer median life. Moreover, it also seems reasonable to project that the distributions at lower voltages would maintain roughly similar spacing as is seen at 500V, 400V, and 325V as long as the percentage of the downward shifts in voltage remains reasonably uniform.

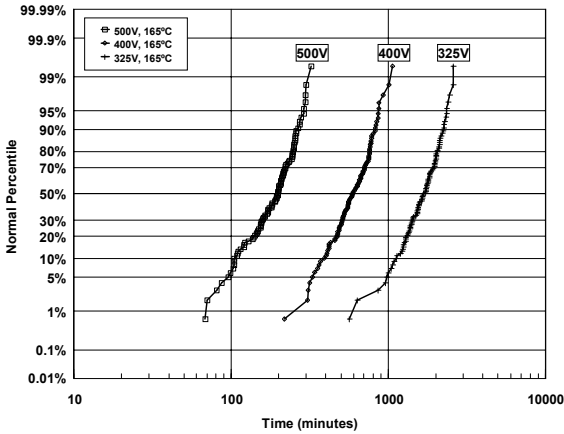


Fig. 3. Lognormal Plot of Failure Percentile versus Time-to-Failure at 325V, 400V, and 500V for Tests Done at 165°C.

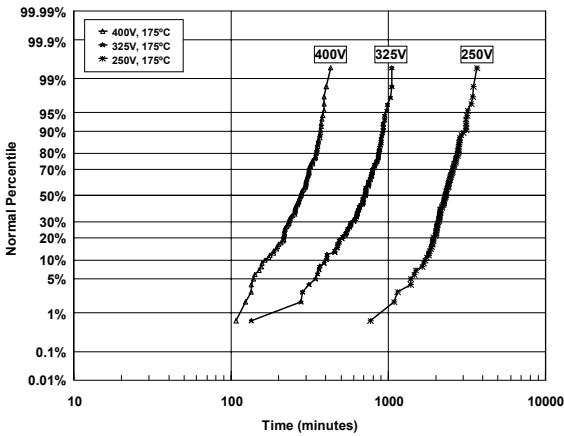


Fig. 4. Lognormal Plot of Failure Percentile versus Time-to-Failure at 250V, 325V, and 400V for Tests Done at 175°C.

Figures 3 and 4 contain the data collected at 165°C and 175°C, respectively. Again, as the voltage is decreased in constant-percentage shifts, the spacing of the failure curves remains reasonably uniform.

Figure 5 is a plot of median life, t_{50} , versus test voltage at 175°C, 165°C, and 155°C. In this figure, each failure distribution discussed above has been reduced to a single statistic, t_{50} , and is plotted on a “log-log” scale that is chosen to linearize the power-law form of the voltage factor in the acceleration equation introduced in the previous section. Three lines were fit to the data points and the equations of the lines appear in the legend. The exponents for these straight lines range from $n=4.5$ at 175°C to $n=5.5$ at 155°C. It is not known whether the range of values observed for the voltage acceleration exponent reflects temperature

dependence of voltage acceleration, experimental error, or some combination of both.

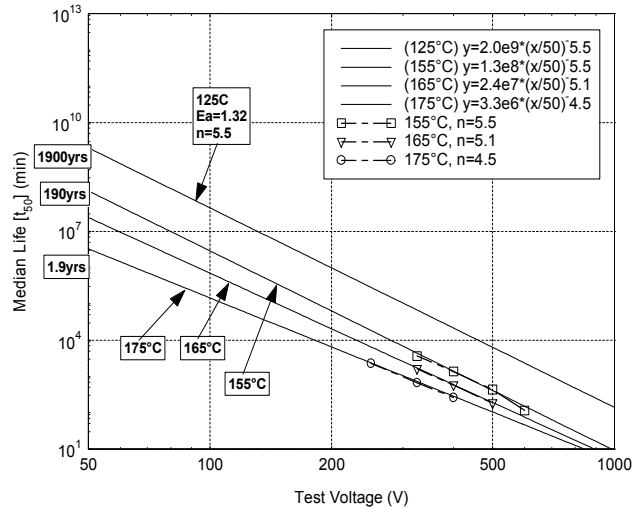


Fig. 5. Plot of Median Life versus Test Voltage at 175°C, 165°C, and 155°C on Log-Log Scale.

The scale for the x-axis was deliberately extended down to 50V, the rated voltage of the test samples. The fitted lines clearly project median lives from several years to hundreds of years at 50V and temperatures between 175°C and 155°C. At this point one might be curious to project the median life that would be expected at 125°C.

It is clearly possible to observe the impact of temperature on median life in Figure 5. The spacing between the lines fit to the data collected at 175°C, 165°C, and 155°C is reasonably uniform and it also appears reasonable to continue this spacing to see what performance is projected at 125°C. A line is included in the figure that is consistent with the known failure data and the choice of $n=5.5$ and $E_a=1.32$ (this value of E_a is consistent with data shown subsequently). This line projects a median life in excess of 1900 years at 50V and 125°C, the maximum rated conditions of the capacitors.

One might also be curious about the expected time until onset of wear-out (versus the time for 50% failures) at maximum rated conditions. In Figures 1-4, the failure distributions generally occupy less than a decade of time. It is thus reasonable to assume that onset of wear-out will occur no more than one-half a decade (roughly a factor of 3) of time sooner than the projected median life. So the data of Figure 5 suggest onset of wear-out sometime after 600 years of service at maximum rated conditions of 50V and 125°C. Even

if these projections were unfavorably in error by an order of magnitude, onset of wear-out would still require 60 years at maximum rated conditions. This is surely a sufficiently long life for all but the most demanding applications.

The preceding discussion has focused primarily on voltage acceleration, but it was possible to project the impact of temperature acceleration by observing the spacing of the lines in Figure 5. Now attention will be focused specifically on temperature acceleration. The same time-to-failure data will be analyzed, but the failure curves will be grouped by voltage rather than by temperature.

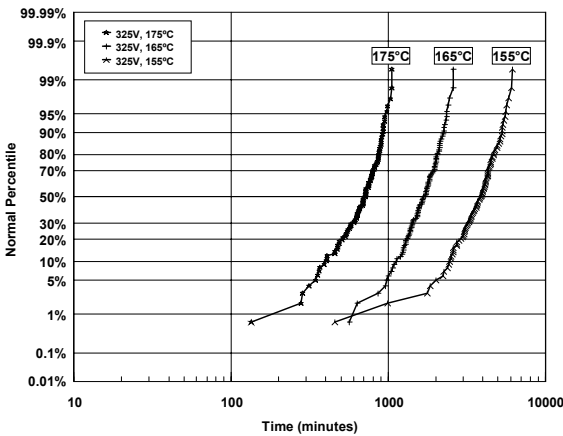


Fig. 6. Lognormal Plot of Failure Percentile versus Time-to-Failure at 155°C, 165°C, and 175°C for Tests Done at 325V.

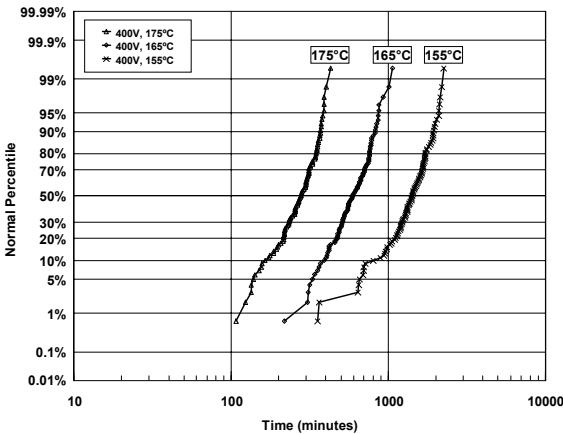


Fig. 7. Lognormal Plot of Failure Percentile versus Time-to-Failure at 155°C, 165°C, and 175°C for Tests Done at 400V.

Data collected at 325V and three temperatures appear in Figure 6. It is clear that the failure distributions are

similar and that the spacing is reasonably uniform as the temperature is changed from 175°C to 165°C to 155°C. It seems reasonable to project that further decreases in temperature would produce failure distributions whose only difference would be longer median life. Moreover, it also seems reasonable to project that the spacing of the distributions at, say, 145°C, 135°C, and 125°C would maintain roughly the same spacing as those seen at 175°C, 165°C, and 155°C.

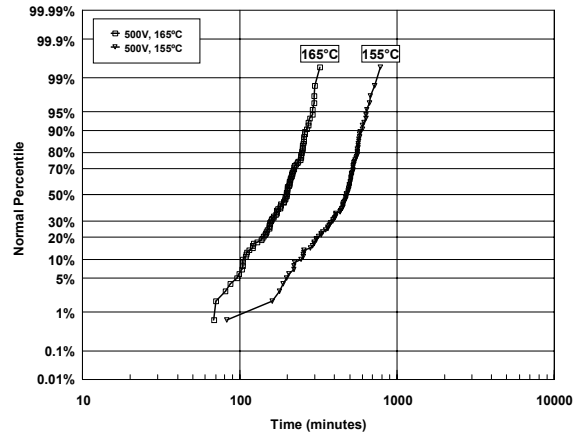


Fig. 8. Lognormal Plot of Failure Percentile versus Time-to-Failure at 155°C and 165°C for Tests Done at 500V.

Figures 7 and 8 contain the data collected at 400V and 500V, respectively. Again, as the temperature is decreased in 10 degree steps, the spacing of the failure curves remains reasonably uniform.

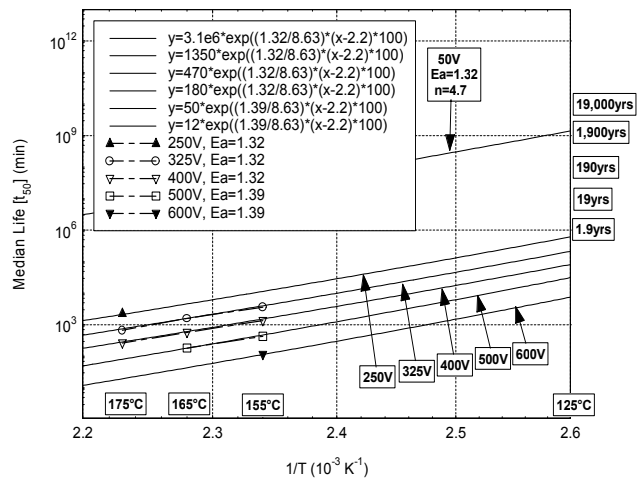


Fig. 9. Plot of Median Life versus Inverse Absolute Temperature at 600V, 500V, 400V, 325V, and 250V.

Figure 9 is a plot of median life, t_{50} , versus inverse absolute temperature at 600V, 500V, 400V, 325V, and

250V. In this figure, each failure distribution discussed above has been reduced to a single statistic, t_{50} , and is plotted on a “semi-log” scale that is chosen to linearize the Arrhenius temperature factor in the acceleration equation introduced in the previous section. Four lines were fit to the data points. The 600V and 250V lines share the slopes of the 500V and 325V lines, respectively, since there is only one data point for each of these voltages. Equations of the all the lines appear in the legend. The activation energies, E_a , for the fitted lines range from $E_a=1.39$ at 500V to $E_a=1.32$ at 325V. This is a much tighter range of values than was observed for the voltage exponent above. These values of E_a are consistent with those reported by others and summarized by Maher³.

The scale for the x-axis was deliberately extended up to $2.6E-3$ inverse kelvins (125°C), the rated temperature of the test samples. The fitted lines clearly project relatively short median lives from about 8,000 to 200,000 minutes (160-3000 hours) at 125°C and voltages between 600V and 325V. However, the projected median life at 325V is still too long to comfortably verify at 125°C , which suggested testing between 155°C and 175°C to keep test time within practical limits.

As was the case with temperature in Figure 5, it is clearly possible to observe the impact of voltage on median life in Figure 9. The spacing between the lines which were fit to the data collected at 600V, 500V, 400V, 325V, and 250V is reasonably uniform, and it also appears reasonable to continue this spacing to see what performance is projected at 50V. A line is included in the figure that is consistent with the known failure data and the choices of $n=4.7$ (conservative estimate at the low end of the range in figure 5) and $E_a=1.32$. This line also projects a median life in excess of 1900 years at 50V and 125°C . Were the voltage exponent to be chosen higher, e.g. $n=5.5$, the projected median life at rated conditions would be even longer.

It is worth noting that a substantial gap exists between the projected line at 50V and the lines that represent testing at 325V and 250V. There appears to be much more room for error in the projection of life at lower voltages than in the projection of life at lower temperatures. Unfortunately, there is no practical way to avoid this uncertainty, but it is comforting that the projected life at maximum rated conditions is far in excess of that necessary for successful application of these devices. Thus there is room for a substantial margin of error.

SUMMARY AND CONCLUSIONS

It has been demonstrated that time-to-failure distributions of multilayer ceramic chip capacitors do not significantly alter their shape even when the applied stress is significantly accelerated during HALT testing. Therefore, one concludes that no new failure mechanisms are activated under these highly accelerated conditions.

Plots of median life versus test voltage and temperature produce families of curves that are proportionately spaced and reasonably linear when appropriately scaled with respect to Prokopowicz' acceleration model. Thus, one concludes that time-to-failure under more normal conditions (at or below maximum device ratings) can be projected with reasonable confidence by applying Prokopowicz' model and values of n and E_a that are derived from accelerated testing of sample populations of those devices.

For the devices tested during this study, projected median life at maximum rated conditions was well in excess of 1000 years, and for some devices, considerably longer. Onset of failures, even after discounting up to an order of magnitude of error in the predictions, was still in excess of 60 years for the KEMET BME ceramic chip capacitors when they are applied at their maximum ratings. Thus, in spite of the existence of an identifiable wear-out mechanism, BME capacitors are shown to have inherent reliability that exceeds the reliability required for almost all conceivable applications.

REFERENCES

- ¹ T. Prokopowicz and A. Vaskas, “Research and Development, Intrinsic Reliability, Subminiature Ceramic Capacitors,” Final Report, ECOM-90705-F, 1969 NTIS AD-864068.
- ² F. Jensen, Electronic Component Reliability, John Wiley & Sons, West Sussex, England, 1995, pp. 8-11.
- ³ G. Maher, “Highly Accelerated Life Testing (HALT) of K-4500 Low Fired X7R Dielectric,” Proceedings of the Passive Components for Power Electronics Workshop, Apr. 26-27, 2000, Penn State University. Also presented in parts at the US – Japan Seminar, Nov. 1999, Okinawa, Japan.