

*This month's Tech Topics describes a recent major contribution to improving the thermal robustness of KEMETMLC chips. We congratulate the team led by Steve Armstrong and Andy Henderson.*

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### **Stress Reduction Improves the Thermal Robustness of KEMET Ceramic Chips**

*by Andy Henderson*

In the continuous drive toward excellence, KEMET's ceramic surface-mount operation has improved chip robustness by a factor of ten every two years. To achieve this improvement in 1991-92, we had to understand and eliminate the root cause(s) of thermal stress failures in chips. However, our very low ppm made it difficult to isolate a defect for this failure mode. This report describes the process the KEMET team followed to isolate and minimize thermal stress.<sup>(1)</sup>

#### **Background of the Problem**

In past improvement efforts, we found that thermal stress failures generally occurred at construction defect sites, no matter how minute. KEMET's board-mount test (BMT)<sup>(2)</sup> - a highly accelerated thermal shock and moisture resistance test - revealed that for this failure mode no construction defects could be found. Analysis of the failures revealed that in many cases thermal shock cracks could not be found, but when the chips were viewed in an optical microscope in dark field mode, light-colored areas were observed. These light areas were always in the active area of the chip, usually adjacent to the side margins near the corners of the active area. Sometimes a crack was observed, typically along the ceramic/electrode interface; occasionally a crack crossed the dielectric layer, connecting opposing electrodes.

#### **Source of Cracking**

We theorized that these light areas and cracks were caused by residual stresses in the chips that led to failure when the chips were mounted and soldered onto circuit boards. Computer modeling of stresses in a chip using finite element analysis supported this theory; the stresses caused by the mismatch in physical properties between the ceramic dielectric and metal electrodes were most intense in the computer model in the areas containing the light color and cracks in actual BMT failures.

Additional support for the theory came when batches of chips were retested several weeks after initial testing.

These batches, which had exhibited no failures during initial testing, experienced some failures during retest, indicating stress relief over time. This confirmation of the stress theory prompted us to investigate the root cause(s) of stress.

#### **Root Cause of Thermal Stress**

Determining the root cause was complicated by the low failure rates of standard product, even under accelerated test conditions. We realized that experimental testing of standard design chips would never produce a response sufficient to reliably determine the root cause(s) of this failure mode. Therefore, we had to learn how to build chips that are highly susceptible to the stress failure mode.

Using the results of the finite element analysis and designed experiments, we designed chips that we have come to call "bricks" (for their thickness). Larger surface-mount chips, such as 1210s, were most susceptible to this problem, especially when they contained a large number of electrodes of thicker than normal construction combined with thin dielectric layers. These "bricks" exhibited typical failure rates of 15 - 30% for this mode. This failure rate was adequate for performing reliable experimentation.

To further ensure the reliability of our test methods, we refined our analytical techniques and developed new methods. Perhaps the most important development was the use of C-SAM (C-mode scanning acoustic microscopy). C-SAM is a non-destructive analysis that detects cracks and other physical flaws inside a capacitor. Refining this technique over time has enabled us to detect extremely small defects or even highly stressed areas that have not yet cracked.

Armed with these tools, we conducted a number of designed experiments to determine those areas of the process contributing to the problem. We examined our process from raw materials through end termination to identify every process variable that could possibly impact stress. Initial experiments confirmed the principles behind the design of the bricks, but did not produce conclusive evidence about the source of stress. There were, however, a number of clues that the key to the problem was in thermal processing of the chips. Further analysis revealed that end termination firing created more stress than any other process step.

#### **Process Improvements**

To understand the stress formation in the end termination firing step, we conducted a series of designed experiments. We determined that the cooling rate had the

greatest effect on stress formation, and that peak temperature was also a critical variable. With this information, we developed a new firing cycle that resulted in better than 90% reduction in stress-related BMT failures in bricks. After confirmation trials produced good results in standard design chips, KEMET implemented the new process in production in March 1992.

### Results and Future Goals

The new end termination firing process resulted in an immediate 90% improvement in the rate of stress-related BMT failures in production chips. The identification of other critical variables resulted in two more significant process changes, implemented in the fall of 1992, that brought the total improvement to 97% as of November 1992 (see Figure 1). Customer feedback has also shown a significant decline in thermal stress-related failures in the field.

Despite the success enjoyed so far, our work is not yet complete. KEMET's goal is the complete elimination of this failure mode with the accelerated test. By March 1993, we will complete additional experiments to reach this goal, which we believe will elevate KEMET ceramic chips to a new level of quality.

- 1 The KEMET team concept is used in continuous improvement projects such as this. The failure analysis techniques were developed and refined by Peggy Bryson and Lynn Day. Steve Armstrong developed the C-SAM analysis technique, and, with Mandy Crowe, performed much of the early experimental work. Andy Henderson and Jeff Franklin developed and implemented the end termination firing improvement process, the subsequent improvements, and are continuing development efforts, and Andy and Jeff receive much assistance from Peggy and Lynn.
- 2 For more information on board-mount testing, see KEMET Tech Topics February 1992 issue.

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**Figure 1.**  
**Involvement in BMT Stress Failures**  
**Resulting from Process Changes**

