KEMET® TECHTOPICS ... THE LEADING EDGE

VOL. 3, NO. 4 • PUBLISHED BY KEMET ELECTRONICS CORP. • P. O. BOX 5928 • GREENVILLE, SC 29606 • (864) 963-6300 • MAY 1993

Surface mount components often start their work history with exposures to highly acid fluxes, molten solder and water jet quenches. This month's Tech Topics discusses a development that increases the robustness of KEMET tantalum chips to moisture-related degradation. The author, Girdhar Arora, was the principal investigator on this project.

Dr. John Piper
Vice-President - Technology

Moisture Barrier For Tantalum Chips

by Girdhar Arora

Introduction

Today's automobiles contain more under-the-hood electronics than ever before, exposing them to high heat and humidity. Manufacturing costs are forcing an increasing number of OEM's to shift their manufacturing facilities to Asian countries where the climate is very humid. Emerging environmental regulations are restricting the use of CFC's for board cleaning purposes. Consequently, the use of ionic fluxes and subsequent hot water washes is becoming quite common.

All of these events place a specific demand on electronic components: moisture robustness. This article describes KEMET's development of a moisture barrier technology that improves the performance of tantalum chip capacitors in humid environments.

Background

Tantalum capacitors in non-hermetic packages are sensitive to moisture. Extended exposure to hot and humid environments can result in elevated DC leakage (DCL). Extensive research at KEMET and other capacitor manufacturers has determined that the transport of ionic species toward the dielectric tantalum pentoxide (Ta_2O_5) layer is responsible for this DCL degradation; moisture simply provides a transport medium for the ionic species.

The nature of these ionic species and the failure mechanism depends on the biasing state of the device during the moisture exposure. In a passive humidity test (no applied voltage), positively charged silver ions migrate toward the dielectric. The source of these ions is the layer of silver-filled conductive paint used to provide contact between the capacitor and its negative leads. In a bias humidity test (tantalum as positive and silver as negative), anions (negatively charged) diffuse toward the dielectric. Examples of such ions are nitrates and chlorides, both of which may be present as impurities inside a tantalum chip. The electric field repels the positively charged silver ions, preventing them from migrating.

Failure Mechanisms

Microscopic flaws (defects) in Ta_2O_5, caused by atomic-level impurities, are responsible for most of the leakage current in a tantalum capacitor. In an operational capacitor, these defects are electrically isolated from the capacitor circuit through a chemical process called "healing." When current flows through a defect, the defect and its surrounding manganese dioxide (MnO_2) become hot. At around 400°C, MnO_2 loses oxygen and converts into highly resistive Mn_2O_3. This conversion plugs the defect, healing the capacitor.

KEMET's research, using model experiments, has established that an increase in DCL of the tantalum chips occurs when both moisture and ions are present and when the latter migrate towards the dielectric, increasing the conductivity of the defect site. Increasing the temperature of a moisture test accelerates the migration process.

Approaches to the Problem

There are three fundamental approaches to addressing moisture-related DCL failure in a tantalum chip:

1. Reduce moisture diffusion
2. Reduce ionic concentration
3. Reduce ionic mobility.

For several years, KEMET has been researching the following alternatives for mitigating the ionic migration problem:

- Sacrificial anode: Silver migration occurs because silver is very electrochemically active. Incorporation of an even more active metal (sacrificial anode) such as copper or zinc into the cathode suppresses the corrosion of silver at the expense of the sacrificial anode. This approach, however, results in increased Effective Series Resistance (ESR) of the capacitor because the corrosion products of sacrificial anodes are more resistive than the corrosion products of silver (copper oxide has higher resistivity than silver oxide).
- Replace silver with palladium: Palladium is higher in the galvanic series than silver and hence does not ionize readily. Its cost, however, is prohibitive.
- Moisture barrier: Incorporate a hydrophobic barrier inside the active capacitor element.

Of the possible solutions studied, the moisture barrier appeared most promising. KEMET pursued development of this technology.

The Solution: Moisture Barrier

Moisture barrier is a novel technology developed at KEMET that significantly enhances the performance of our tantalum chips. Conceptually, it is somewhat similar to the idea of treating a rug with Scotchguard®. It reduces moisture and ionic diffusion toward the dielectric, thus preventing an increase in leakage current.

The moisture barrier is applied and then treated at an elevated temperature. The barrier fills the porosity in the capacitor and modifies the surface chemistry of the underlying layers, restricting the diffusion of water molecules and ionic species. Figure 1 shows a cross-section diagram of tantalum chip with the moisture barrier.

The location and properties of the moisture barrier are critical. We had to stop moisture and ionics without impeding the free flow of electrons. Restricted electron flow reflects as increased EST of the capacitor.

A. Development

To develop this technology, we followed the KEMET Advanced Quality Planning System. First we identified the customers and their needs. In this case, there were two sets of customers: the external customers who would use the capacitors and appreciate their robustness, and the KEMET manufacturing plant personnel who would use the process and materials resulting from the development.

We met with plant personnel and with KEMET's tantalum chip product managers, who represented external customers. Together we established customer needs and then used Quality Function Deployment to translate those needs into design requirements.

We used designed experiments to evaluate the performance of a large number of materials. Accelerated short-term moisture tests such as pressure cooker (121°C, saturated condensing steam) and HAST (121-150°C, 85%RH, non-condensing steam) were used to assess the effectiveness of various materials and process combinations. After the moisture tests, DCL and ESR were analyzed for statistically significant effects. After several rounds of experimentation, a formulation was developed that satisfied the design objectives.

In parallel with the moisture barrier material development process, we established a correlation between the short-term moisture tests and long-term reliability tests such as load humidity (85°C, 85%RH, V_r) and passive humidity (85°C, 85% RH,0VDC). We designed an empirical model to predict long-term performance using short-term data, which significantly reduced our evaluation and development cycle time.

B. Reliability Testing

We performed the following long-term reliability tests on tantalum chips with moisture barrier technology:

Reliability Test	Time
Life Test @ 85°C/V rated	4000 hrs.
Life Test @ 125°C/V 2/3 rated	4000 hrs.
Storage Life @ 150°C/(0VDC)	1000 hrs.
Extended Thermal Shock (-55°C to 125°C)	1000 cyc.
Resistance to Solder Heat (300°C/1 min)	1 dip
Temperature Stability (-55°C to 125°C)	1 cycle
Moisture Resistance	42 days
Passive Humidity (85°C/85%RH/0VDC)	1000 hrs.
Load Humidity (85°C/85%RH/Vrated)	1000 hrs.

C. Production Implementation

Scale-up of the moisture barrier process from bench level to production was a team effort from KEMET's Technology, Equipment Engineering, Quality Assurance and Safety departments, as well as from the Mauldin plant that manufactures tantalum chips. Before production implementation, the team performed optimization, control system development, equipment fabrication and installation, manufacturing documentation, and safety audits.

Much before production implementation, the team completed Failure Mode and Effects Analysis (FMEA) of the process. FMEA is designed to anticipate various failure modes and build robustness in the product and processes at the design stage. FMEA helps reduce cycle time and costs.

Performance Enhancement

The moisture barrier has significantly enhanced the performance of KEMET's tantalum chip product in several areas. As Figures 2 and 3 illustrate, it has improved DC leakage levers of tantalum chips after passive humidity test (85°C, 85%RH, 0VDC) and moisture resistance test (Mil-Std 202, Method 106).

In addition, the moisture barrier significantly improves the wet surge performance of the tantalum chips. It also stabilizes the capacitance, dissipation factor, and ESR after life tests (85°C and 125°C).

Moisture barrier development is an example of a customer-driven program at KEMET that raised the performance level of our tantalum chips in humid environments. This technology has helped us develop a more robust product that better meets the needs of our customers.

Figure 1
Cross-section of tantalum chip with Moisture Barrier

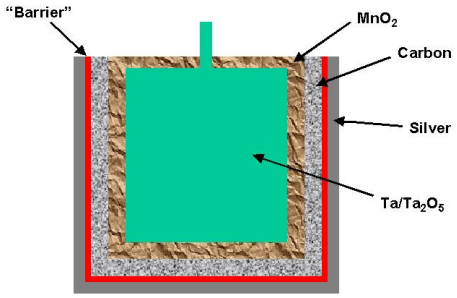

Figure 2
Passive Humidity Test - 1000 Hours
85°C, 85%-RH, 0 VDC

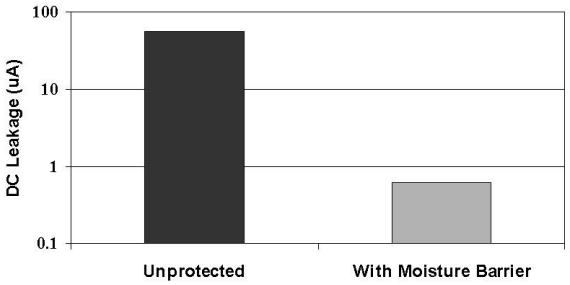

Figure 3
Moisture Resistance Test - 42 Cycles
Mil-Std 202, Method 106