Thin Film MLCC

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Abstract

An ever-increasing need for higher capacitance per unit volume multilayer ceramic capacitors (MLCC) has lead to dielectric thicknesses and internal electrode thicknesses in state-of-the-art MLCC below 1 μm using traditional thick film MLCC manufacturing technologies. Traditional MLCC manufacturing technology has surprisingly evolved to this level of capability and beyond. The topic of how thin this technology can go has been the subject of much debate. This paper discusses the state-of-the-art of traditional MLCC technology and compares this technology to potential thin film manufacturing techniques for MLCC. The practicality of thin film technology for MLCC manufacture is discussed with respect to materials sets, potential fabrication technologies and associated limitations, and design philosophies. Also considered are the impact of general trends in the electronics industry, anticipated evolution of MLCC form factor and general device requirements with respect to thin film technology as a potentially viable future MLCC fabrication method.

Introduction

A constant driver for the electronics industry is to add more functionality in less space. This has resulted in a relentless effort to increase the volumetric efficiency (VE) ceramic capacitors (MLCC). Figure 1 illustrates the increase in capacitance and VE of 0603 (1608 metric) MLCC since ca. 1994. The increase is well fit by a relation indicating that, for the 0603 case size, maximum available capacitance and VE have increased, over time, at a rate that exceeds that of Moore's law, doubling approximately every 13 to 14 months (compared to ~18 months for Moore's law).[1] In order to achieve this impressive rate, all design parameters for MLCC have evolved over time. Figures 2-4 illustrate the estimated and projected evolution of the major design parameters for MLCC in order to achieve the rate depicted in figure 1, using capacitance and VE equations and assuming dielectric constant (K) is held constant at 3500.[2] Figure 2 indicates that the largest contribution to the rate of increase in VE and capacitance in MLCC is the combination of reducing dielectric thickness and increasing active count.

As with Moore's law in the IC industry, there is much speculation as to when current MLCC materials and production technologies will "run out of gas." The basic process for making MLCC has not changed appreciably in more than a decade and it is difficult to imagine standard suspension coating processes capable of manufacturing dielectric films that will fire to less than 170 nm (as is projected for 2010 in figure 2) at a production scale having active layer counts of ca. 1,900 in an 0603 case size with an acceptable yield.

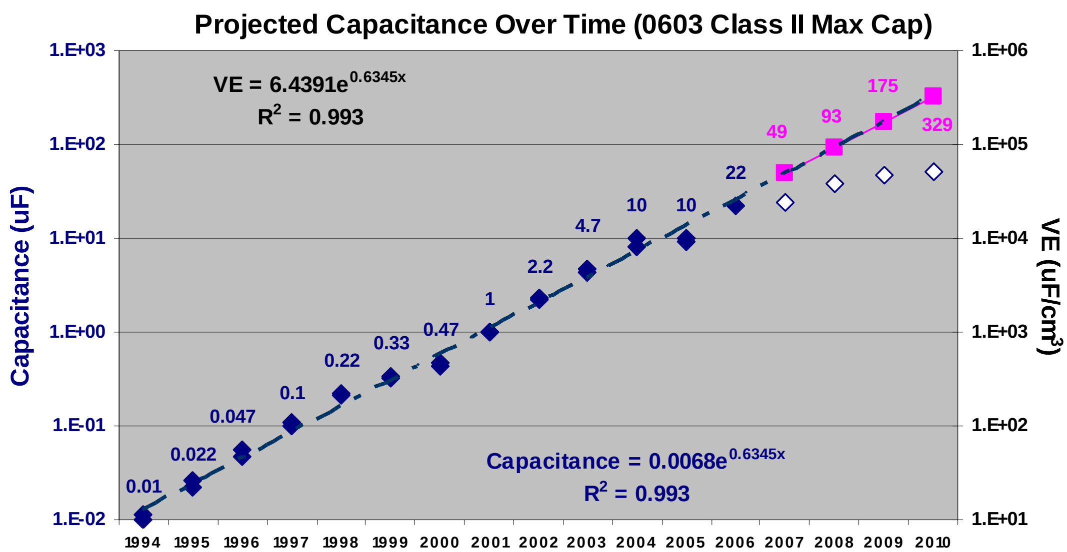


Figure 1. Evolution and projection of capacitance and VE with time, 0603 class 2 MLCC

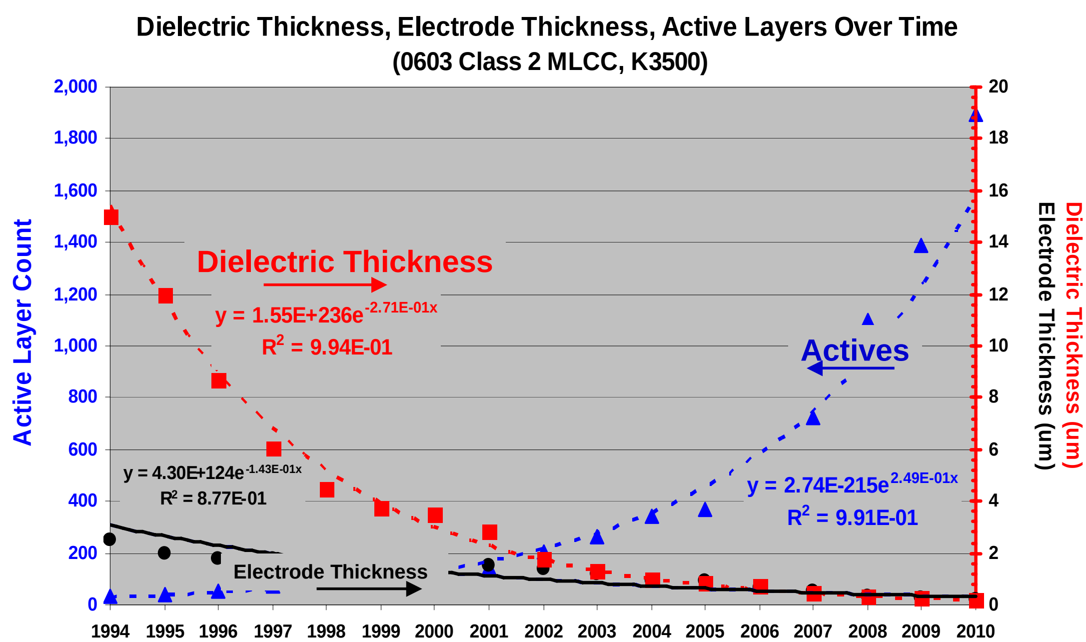


Figure 2. Evolution and projection of dielectric thickness, electrode thickness and active layer count over time 0603 class 2 MLCC

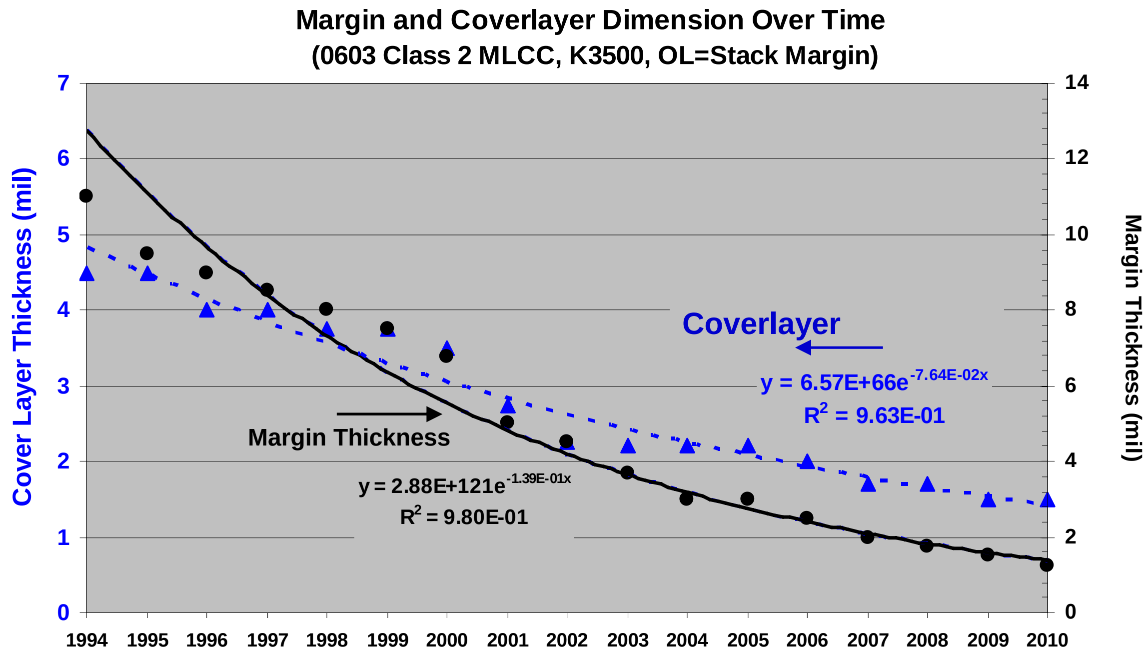


Figure 3. Evolution and projection of cover layer and margin dimensions with time, 0603 class 2 MLCC

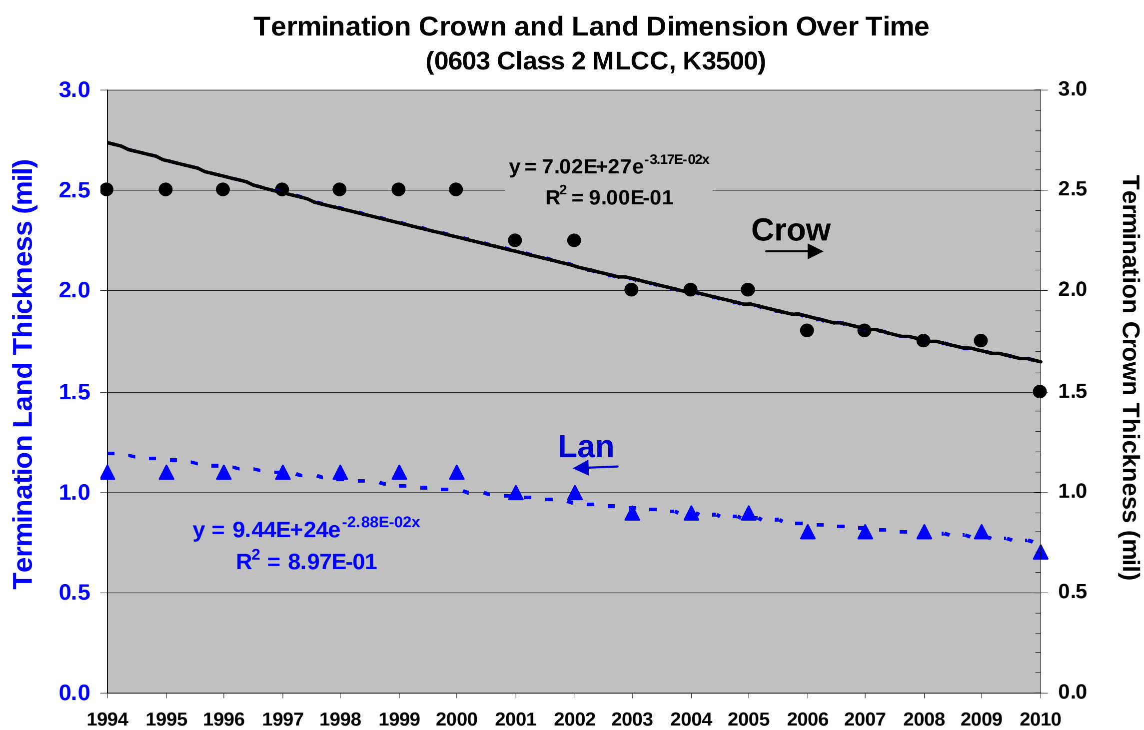


Figure 4. Evolution and projection of termination dimensions over time, 0603 class 2 MLCC

Additionally, these calculations and projections have been performed using the assumption that K has not and will not change appreciably with time (or dielectric thickness). While K has not largely changed in the past for commercial class 2 dielectrics, due to successful development efforts, as well as a transition from X7R to X5R dielectrics, etc., it is doubtful that this trend will continue going forward as dielectric thickness decreases appreciably below ~0.8 µm. The generally accepted reason for this doubt is that the dielectric used needs to have several grains throughout the thickness of each dielectric layer in order for these $BaTiO_3$-based class 2 dielectrics to be suitably reliable. While the number of grains per layer has also decreased with time, it is likely that, unless a break-through technology in dielectric materials is introduced, the number of dielectric grains per layer will not go below ~4 by the year 2010. With that considered, the projected dielectric grain size will need to dramatically decrease in order to achieve the dielectric thickness goals projected as indicated in figure 5.

It is generally understood that K decreases as grain size is reduced below ~1 µm.[3] Figure 6 illustrates K vs. average grain diameter. Thus, K is anticipated to decrease in class 2 dielectrics as dielectric thickness is reduced as projected in figure 7. It should be noted that the extent of these projections is subject to debate as scientists have reported the ability to synthesize dense $BaTiO_3$ exhibiting average grain size as low as ca. 8 nm while preserving K as high as ~1,800.[4] Regardless, if $BaTiO_3$-based dielectrics continue to be used in MLCC, K is anticipated to decrease as dielectric thickness decreases in order to increase VE to keep pace with the "MLCC curve" depicted in figure 1. If K is reduced with grain size as indicated in figure 6 and all other design factors remain as projected, the VE and capacitance curves will fall off from the exponential projection as indicated by the white diamonds in figure 1 (note: the solid squares in figure 1 are projections are for K unchanged and represent the best case scenario), requiring even more aggressive MLCC design parameter goal advancement than indicated in figures 2-4 in order to meet the "MLCC curve" in figure 1.

It may be possible to negate this effect somewhat with suitable dielectric formulation. For example, it may be possible to increase room temperature K at the expense of loss in K at -55C (rarely needed for portable electronic devices) for example. Also, alternative materials may be developed, such as relaxor dielectrics, although they are typically Pb-containing and have been avoided by most major MLCC manufacturers for various legal and environmental regulatory reasons.

From the above discussion, it is evident that traditional MLCC materials and fabrication technologies will be very hard-pressed to keep pace with the "MLCC curve." MLCC with dielectric thickness of less than 0.2 µm, combined with more than 1,800 active layers and manufactured with high yield, excellent reliability and competitive cost, and produced using traditional materials and MLCC fabrication technology are difficult to fathom. If traditional MLCC materials and fabrication technologies begin to lag the "MLCC curve," the opportunity will arise for the emergence of disruptive technologies. Multilayer thin film technology has long been suggested as the next technology for MLCC, displacing traditional MLCC technology for high VE manufacturing. This anticipation is yet to be realized however. Thin film processes have associated fundamental limitations with respect to multilayer structures. This paper discusses thin film technology with respect to MLCC.

Discussion

A great deal of development effort has been expended upon development of thin film MLCC with limited success. Thin film deposition techniques evaluated to date have run myriad techniques such as sputtering, thermal evaporation, spin coating, ink jet deposition, electrophoretic deposition, aerosol deposition, anodization, and the like. As an example of a thin film MLCC device, figure 8 illustrates a thin film MLCC fabricated using spin coated sol gel $BaTiO_3$ (ca. 200 nm thickness) for the dielectric, combined with sputter coated Pt (ca. 60 nm thickness) for the electrode.

Thin film processes have inherent advantages over standard MLCC "thick film" technology, such as the ability to deposit extremely thin, uniform, flaw free films. Additionally, thin film processes are amenable to high resolution patterning using photolithography or the like, enabling the production of structures with very fine spatial detail.

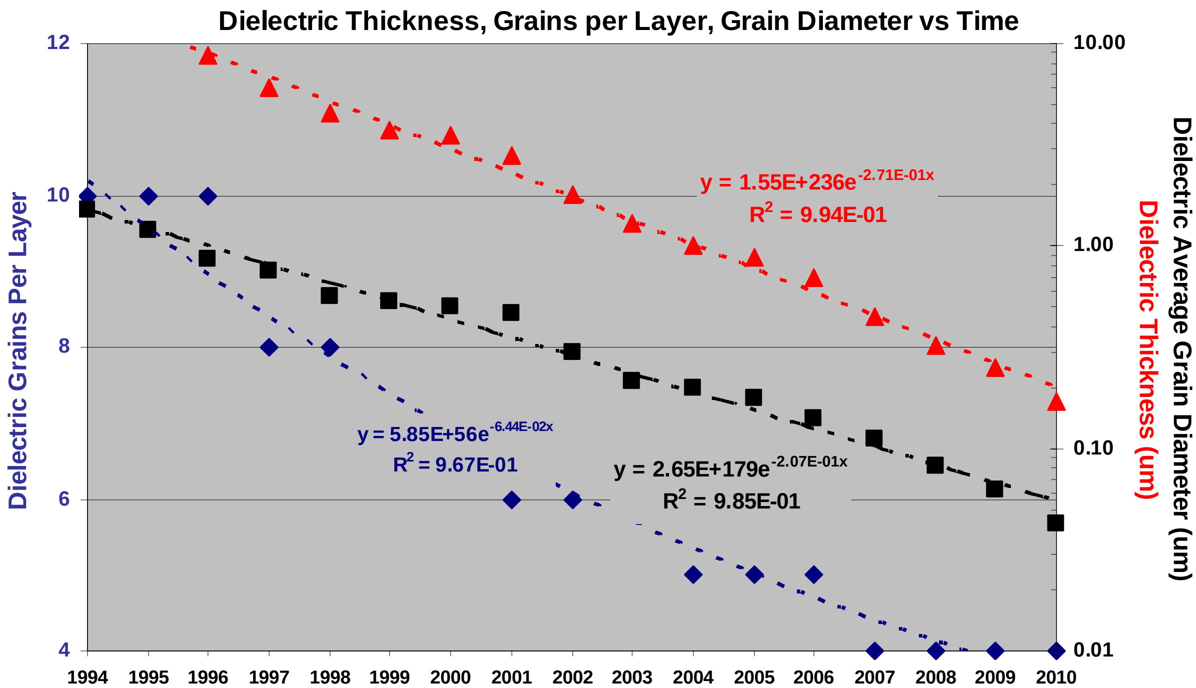


Figure 5. Evolution and projection of dielectric thickness, number of grains per layer and average grain diameter vs. time

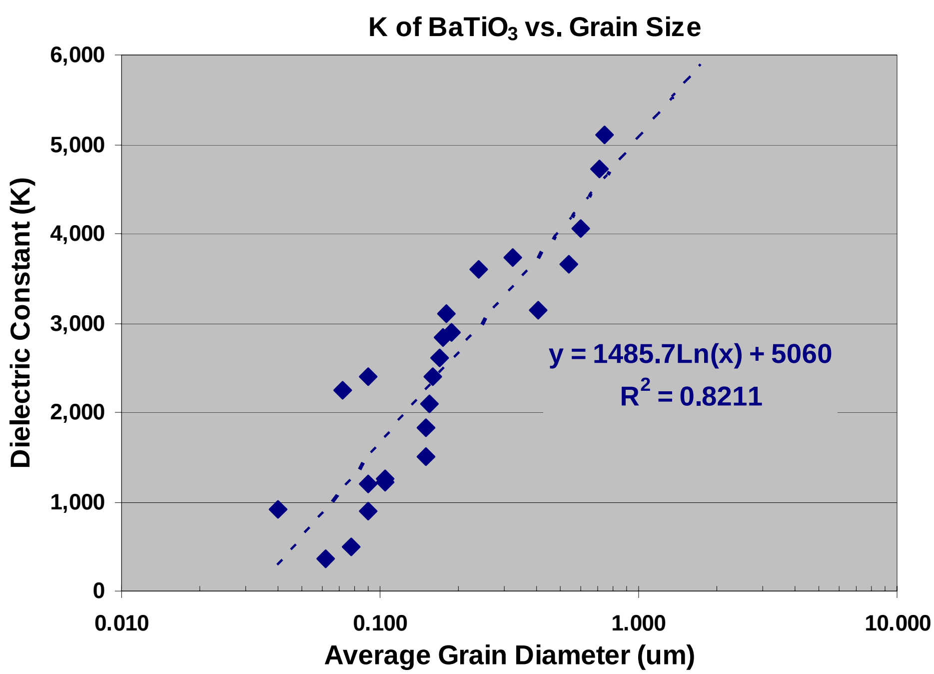


Figure 6. K of $BaTiO_3$ vs. average grain diameter [5]

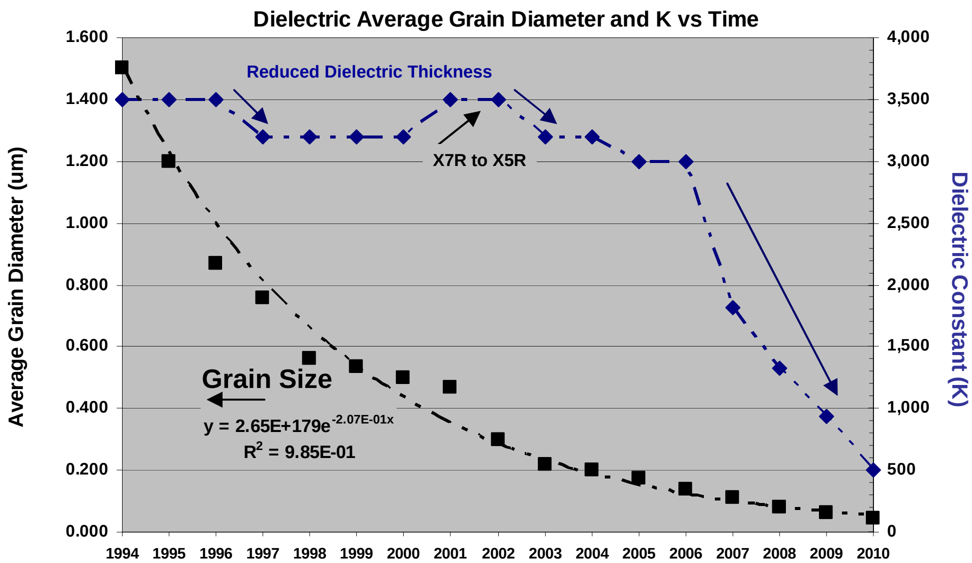


Figure 7. Evolution and projection of grain size and K for class 2 dielectric vs. time

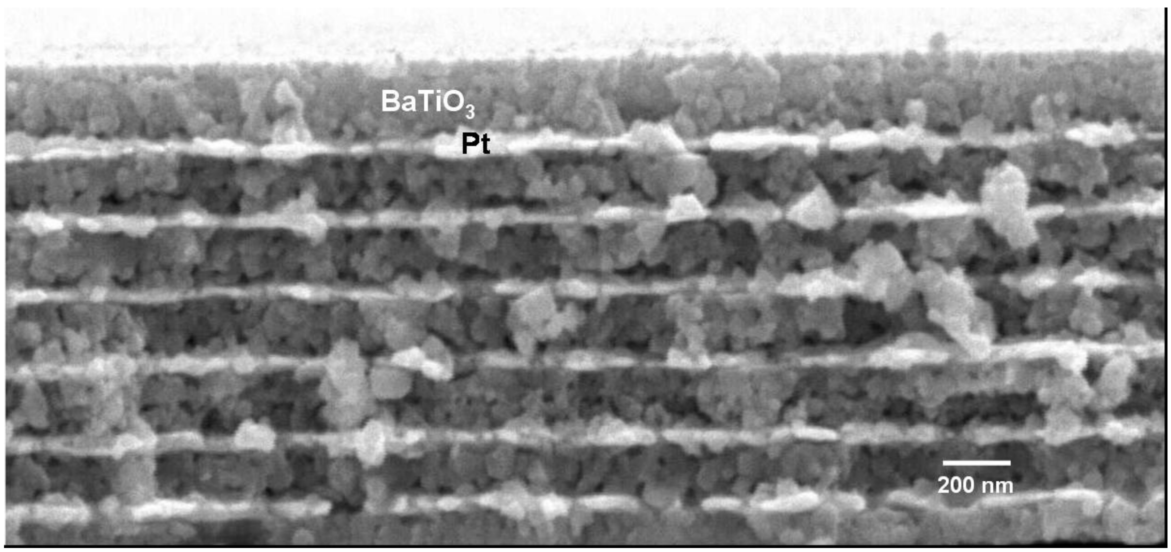


Figure 8. Thin film multilayer structure fabricated at Penn State University

Perhaps the greatest limitation of thin film technology is that it is very difficult, if not prohibitive, to develop thin film systems with very high layer counts. Thin film deposition rates are typically slow (on the order of minutes per micron). Additionally, thin film ceramic systems typically must be thermal processed every few layers, as cofiring of the entire monolith (~1,800 or more layers) in this case results in venting or shrinkage cracks, or other catastrophic flaws, due to the relatively large shrinkage and shrinkage mismatch of the dielectric and the metal during sintering and densification processes. These factors may result in exceedingly long process times for thin film MLCC manufacturing as compared with traditional MLCC.

As an example comparing the relative rates of MLCC structure build-up of thin film MLCC vs. traditional MLCC, the time to build a "pad" of MLCC may be estimated for both processes, assuming that physical vapor deposition (PVD) or chemical vapor deposition (CVD) processes are used to manufacture the thin film MLCC and the deposition rate of both the thin film dielectric and metallization is 1 μm/minute. Additionally it is assumed that the build-up portion of the process is the rate limiting portion of the process, and that the built up "pad" would be thermal processed after deposition of every 5 active layers (dielectric plus electrode) using a rapid thermal annealing (RTA) process which accomplishes thermolysis and densification in 1 minute with transition times of 20 seconds for each step interchange. It should be noted that the above numbers are quite optimistic and are considered to be a best case for thin film multilayer manufacturing technology.

For the case of 0603 MLCC in the year 2010 (1,800 active layers comprised of 0.17 µm dielectric and 0.20 µm electrode metal) and not including cover layers, this scenario would take ~20 hours to create one "pad" worth of capacitors, while it would take ~2.5 hours to make one "pad" worth of MLCC using traditional techniques assuming a 5 second cycle time for electrode printing and for printed sheet stacking and that both processes are done in parallel. The estimated throughput difference between thin film and traditional techniques in the above example mandates that the format of the thin film "pad" of MLCC be ~8 times the area of the traditional MLCC "pad" in order to have similar throughput. Assuming a 12" x 12" pad for the traditional approach, this example requires that the thin film approach have a format of ~33" x 33" in order to have about the same throughput. While this is not prohibitive, it would certainly require very expensive production equipment. Additionally, a process with the capability described remains to be developed. It is likely that this system would have prohibitive preventive maintenance issues and significant yield issues as well.

A second issue is that the MLCC must be built up on some type of substrate. In the case of traditional MLCC manufacturing, that substrate is typically removed during green processing. With thin film processes, it is not obvious as to how to make the substrate removable. Regardless, unless the substrate is removable, it will take away from the active volume of the MLCC device. The thinnest substrates available are typically about 0.005" to 0.010" in thickness. In the case of the year 2010 0603 case size target device (i.e., cover layer dimensions of 0.0015" each for a total cover layer dimension (top and bottom) of 0.003"), the substrate would account for about double of the total targeted cover layer dimension, forcing a significant reduction in dielectric thickness or electrode thickness in order to maintain VE and capacitance within the package. In the case of an 0201 or 01005 case size MLCC, the addition to the device thickness by the substrate would be prohibitive because the total allowed thickness of the thin film MLCC device would be consumed by substrate. Thus, it will be necessary to develop a manufacturing process that utilizes a removable substrate as with traditional MLCC manufacturing techniques, in order to use thin film manufacturing processes for the smallest case size MLCC.

Another consideration is materials and process cost. Thin film multi-layering processes tend to use relatively expensive materials systems and can be quite wasteful with respect to materials usage as the reactor tends to get coated with the materials (waste) and the materials utilization efficiency for the chemical reaction is low. While efforts have been directed toward development of low cost electrode materials as illustrated in figure 9, it is very likely that the materials portion of a thin film MLCC device cost will increase significantly compared to traditional MLCC. These factors combined will make it extremely challenging for thin film MLCC to be cost competitive with traditionally processed MLCC.

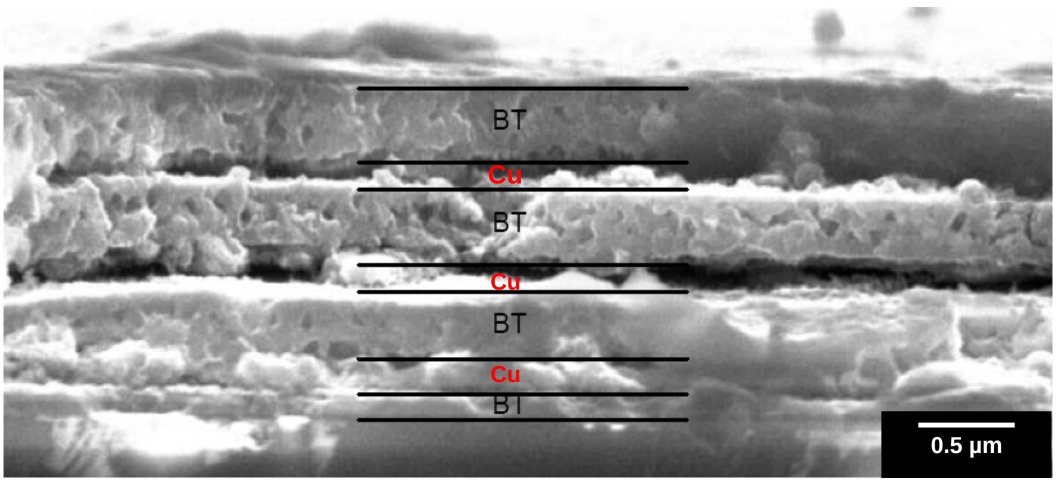
Regardless of MLCC manufacturing technology, very substantial materials development will be required in order to keep pace with the "MLCC Curve." The challenge of maintaining K has already been discussed. Other challenges reside in the ability of high K dielectric materials to accommodate electric field. As a "rule of thumb," MLCC voltage rating is established at about 10% of the breakdown voltage of the MLCC of interest. For example, a 6.3 V device will typically have an upper voltage breakdown (UVBD) of >63V. State of the art 6.3 V devices are currently available with dielectric thickness on the order of 0.8 µm to 0.9 µm. That means that the breakdown voltage of the dielectric used needs to exceed a minimum of ~80 V/µm. Typical devices actually exhibit UVBD values exceeding 140 V/µm to 150 V/µm in order to ensure adequate reliability, combined with adequate yield. Assuming that MLCC design for voltage rating is directly proportional to dielectric thickness, the 0.17 µm dielectric thickness MLCC device designed for year 2010 would have a voltage rating of ~1.33 V, limiting it from use in all but low voltage microprocessor applications.

The above example assumes an X5R dielectric system with maximum use temperature of 85C. As the industry moves toward higher temperature applications (e.g., X6S or X7?), voltage ratings will need to decrease even further (as much as 25 to 50% assuming activation energy for dielectric wear out on the order of 1.1 eV).

Combined, these factors will lead to a rated voltage for the year 2010 maximum capacitance MLCC device of less than 1 V. Therefore, materials development, focused toward increasing reliability of high K dielectrics is warranted. It is likely that this development will be necessary regardless of whether traditional or thin film MLCC fabrication technique is used for MLCC manufacture. Thin film development efforts will not necessarily adequately address reliability requirements and the challenge of decreasing K with decreasing dielectric thickness without parallel development efforts targeted specifically to address these issues. These issues will continue to be a challenge for traditional MLCC manufacturers as well.

Materials development will also be necessary with regard to engineering of the dielectric – electrode interface. As dielectric thickness is reduced, the insulation resistance (IR) of the resulting MLCC device becomes more and more dependent upon insulating properties of the dielectric – electrode interface.[6,7] Thus it will be very important to properly engineer the dielectric - electrode interface regardless of build-up technique and precursor material configuration. Development will likely focus on maximization of the electrode work function, as well as on the formulation of the dielectric material in order to maximize the insulating properties: more importantly, the insulating properties of the dielectric and dielectric – electrode interface.

Cofired Multilayer Thin Film Structure (Cu/BT)



Courtesy of PSU: Patent Pending

Figure 9. Thin film MLCC with Cu internal electrodes, fabricated at Penn State University

Based upon the above arguments it not likely that thin film manufactured MLCC will displace MLCC manufactured utilizing traditional techniques any time in the near future. Yet, the ability to form very thin, uniform layers of dielectric and/or electrode, afforded by thin film manufacturing processes, is very attractive to the MLCC and the capacitor industry in general, and many significant development efforts have been generated with this focus[8,9,10,11]. The challenge is how to best maximize the active area per unit volume within the device utilizing a process that imparts a thin, uniform, flaw free, high K, dielectric film in a cost effective manner.

Many thin film techniques enable uniform coating of a large area with relative ease, and with low cost. Anodization, electrophoretic deposition and dip coating, or micropad stamping of sol gel materials,[12] ink jet deposition[13] and the like, are examples of these types of thin film processes. Tantalum, niobium, niobium oxide and other valve metal capacitors take advantage of this type of coating, utilizing anodization. However, the resulting dielectrics have relatively low K values compared with $BaTiO_3$-based dielectrics (ca. 50 or less vs. ca. 500 or more).

Several patents have addressed deposition of high K dielectrics in the structure of a porous body using either hydrothermal deposition, electrochemical reaction of a precursor solution or impregnation with a precursor or the like.[14,15,16] These methods, while showing promise from a fundamental perspective, have yet to achieve commercial success. It is likely that these processes are limited in that it is extremely difficult to deposit flaw free film over the relatively tortuous interior of the substrate. Work is currently ongoing to take advantage of the healing properties of anodized films in valve metal capacitors, combined with a high K film.[17] The composite material resulting from this hybrid film fabrication approach is illustrated in figure 10. Initial trials have been successful in producing improved VE structures, exhibiting reasonably low leakage currents as compared to standard tantalum capacitors having similar VE.

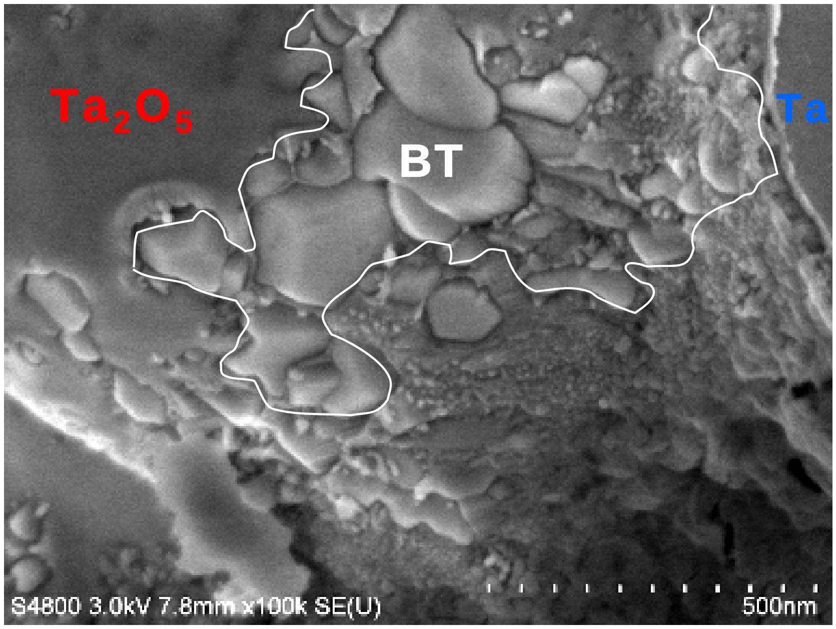


Figure 10. Hybrid tantalum barium titanate capacitor structure

While much development work remains, this composite dielectric structure shows promise with respect to achieving very high VE potential in a relatively easy-to-manufacture capacitor system. With successful development, these high K thin films could be utilized in myriad structures, optimized for maximum surface-area-to-volume. Some potential examples are illustrated in figure 11. These solutions for bulk capacitance with maximized VE will likely have higher ESR than a traditional interleaved MLCC structure. Successful development of these non-traditional structure capacitor systems should enable very high VE embedded capacitance in circuit boards, thereby reducing the need for surface mounted discrete capacitors.

Thin film MLCC designed with the traditional interleaved electrode – dielectric structure may be useful for applications involving high frequency as these MLCC will have low profiles with high capacitance density. These structures, either as surface mounted discrete devices, or as devices printed or deposited to the surface of a circuit board, or active device, may enable enhanced functionality in a small foot print and at relatively low cost. For example a 1 mm footprint thin film MLCC with 5 $BaTiO_3$ layers of K = 1,000 and 150 nm dielectric thickness, with 25 µm stack and overlap margins, and with 150 nm electrode thickness should provide a capacitance of >250 nF (~25 µF/cm^2) in a device height of less than ~5 µm. This type of capacitance density should be more than suitable for most high frequency applications.

For these applications, it is very important to achieve the targeted capacitance value with great accuracy and repeatability. In order to achieve these goals, it is paramount that the deposition technique utilized exhibit high precision of deposition. Micropad stamping shows promise for accurate deposition of thin film materials.[11,12] Figure 12 illustrates the spatial capability potential for micropad stamping. This deposition method exhibits excellent edge resolution and print quality with relatively consistent deposition thickness as indicated in figure 12. This method should be suitable for fabrication of MLCC with traditional interleaved structures of a few active layers (likely <~10). With development, these structures may not need to be trimmed to achieve very consistent capacitance values (e.g., target +/- 1% or better).[9,18]

From the above, it appears that thin film technology will not likely supplant traditional MLCC technology. It appears that thin film technology will be utilized in concert with new structures in order to address future demand of the very high VE application portion of the capacitor industry. Additionally, it appears that thin film technology will be useful for the manufacture of embedded or integrated MLCC of only a few layers (ca. 10 or less), most likely for high frequency applications. Regardless, thin film materials technology will face similar challenges to those currently faced by traditional MLCC technology, including reduced K with decreasing dielectric thickness, reliability challenges at voltage and temperature, capacitor properties challenges with increasing electric field and frequency (e.g., voltage coefficient of capacitance, piezoelectric sound emission, etc.), cost of manufacture, and the like.

Summary

The rate of increase in capacitance and VE for ceramic MLCC has been impressive. Maximum capacitances available have doubled about every 13-14 months, outpacing Moore's Law for IC development. Soon, however, it is likely that MLCC technology will begin to lag the "MLCC curve" due to fundamental limitations of traditional MLCC processes, combined with a fundamental reduction in K observed in thin layer, fine grained barium titanate based ferroelectric dielectrics.

Thin film technology has long been considered the next technology for MLCC. However, thin film technology has fundamental limitations with respect to manufacture of high layer count devices. Additionally, thin film high K dielectrics are subject to the same reduction in K as experienced with thick film based high K dielectrics. Thus, new capacitor structures need to be considered for maximization of VE for bulk capacitance that enable high VE without the associated costs and limitations of multilayer thin film processes. These structures will likely include impregnation of a complex, porous structure. Additionally, a hybrid impregnation and anodization process will likely be used in order to achieve capacitors comprised of thin dielectric films with relatively high dielectric constant and robustness required in commercial capacitor devices produced in a manner that is economically viable.

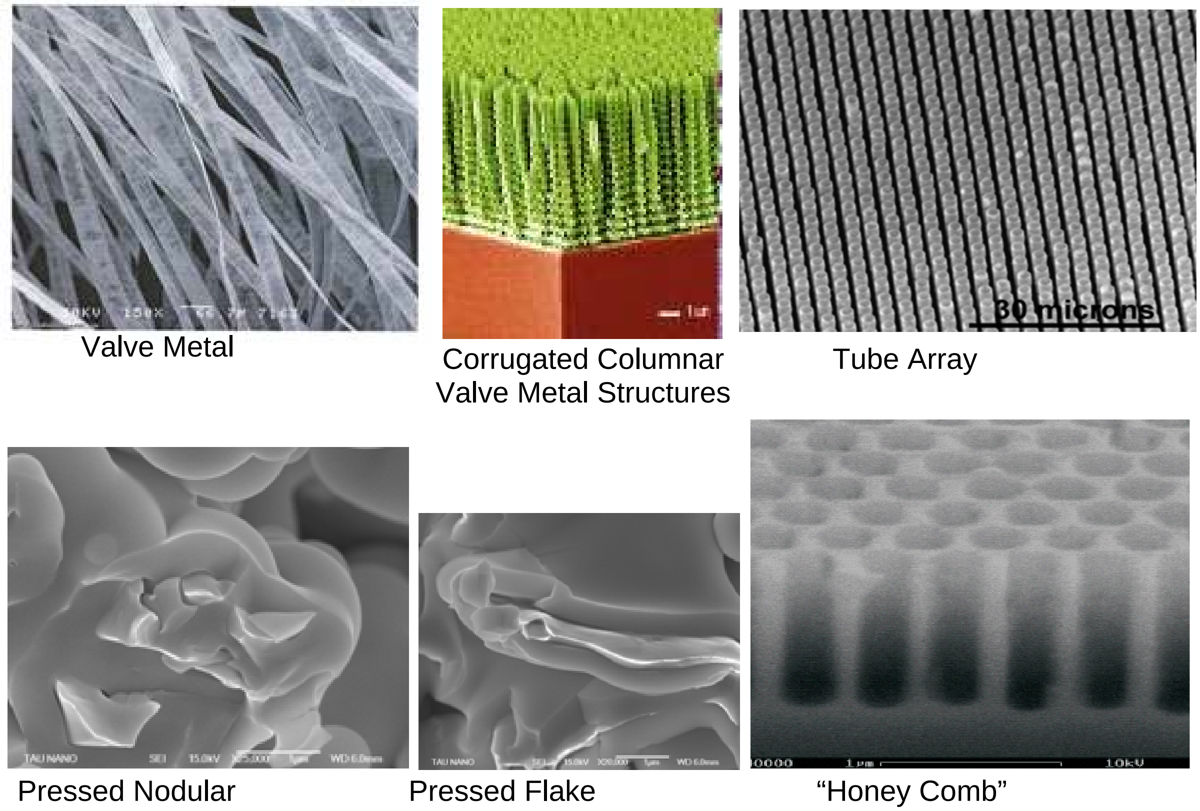


Figure 11. Porous microstructures targeted toward maximizing surface area per unit volume in an open pore structure

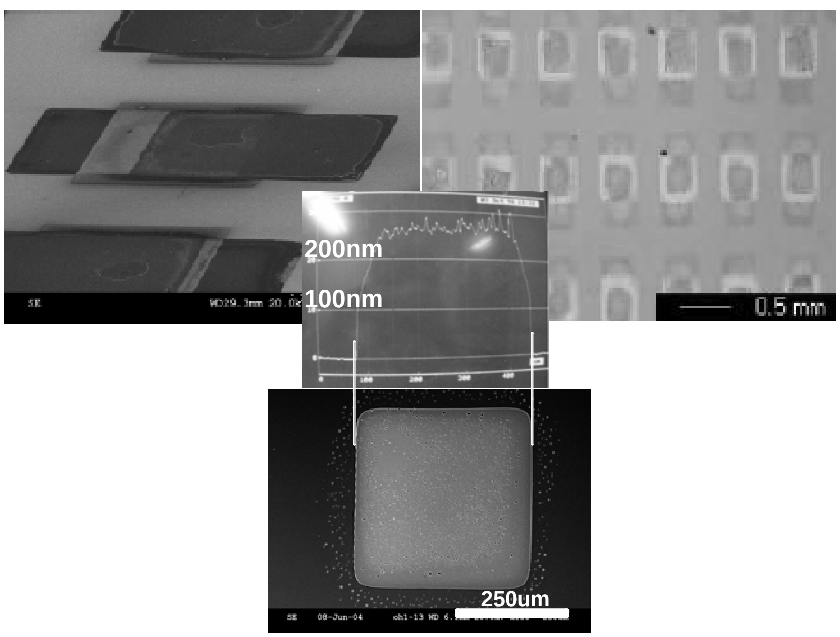


Figure 12. MLCC produced via micropad stamping of a $BaTiO_3$ precursor solution at Penn State University

For design of MLCC for high frequency applications, it is likely that embedded single layer or low layer count MLCC structures will be used. For mid VE applications, it is likely that MLCC will continue to be the best, most economically viable solution.

Very significant materials development will be required in order to have materials suited to MLCC having dielectric thickness less than ~200 nm. Preservation of K will be a major challenge as will developing the insulating properties of the dielectric-electrode interfaces to a level such that extremely thin dielectric layer capacitors exhibit suitable reliability and non polarity. Additionally, development is required in order to increase the dielectric breakdown strength and IV characteristics to levels currently greater than exhibited in traditional high VE MLCC.

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