D-Pack 3D Interposer Decoupling System

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Abstract

D-Pack three-dimensional interposer decoupling system presents a new and fundamentally improved design for high-speed microprocessor decoupling schemes. D-Pack is intended for the decoupling needs of today’s most advanced microprocessors. The base element of the D-Pack is a low inductance, multi-terminal, multilayer capacitor (MLCC) or D-Stick™. D-Sticks may be combined in numerous configurations to form D-Packs suitable for myriad microprocessor designs. In addition to the decoupling function, D-Pack also provides for power and ground feed circuits between the microprocessor package and the parent circuit board. D-Pack is advantageous in that it eliminates appendage circuitry and the associated parasitic inductance, typical of topside decoupling schemes, while enabling a reduced package footprint combined with enhanced thermal management relative to bottom side decoupling schemes. Each D-Stick™ within a D-Pack also serves as an effective feed through filter capacitor as well as providing an excellent thermal conduction path between the microprocessor package and the parent circuit board. D-Pack offers a unique combination of high capacitance density, low inductance, low ESR, nearly perfect noise filtering, and enhanced thermal management in a space saving design. Capacitance densities are available in excess of 1,000 µF/in² (≈150 µF/cm²). Equivalent series inductance (ESL) values of 1 pH or less, combined with power noise filtering with a maximum insertion loss (IL) of nearly 120 dB are possible. D-Pack designs may enable a significant reduction (<25% or more) in package footprint as well as enhanced thermal performance.

Introduction

Use of decoupling capacitors in the electronics industry is ubiquitous as integrated circuits (IC) typically need decoupling in order to work properly. Decoupling requirements have evolved. A typical decoupling scheme has several levels of decoupling capacitors between the power supply and the distance from power supply to the IC or microprocessor is traversed. Decoupling capacitors are typically placed between power and ground local to the IC in order to ensure relatively smooth voltage with respect to time as the IC (typically a microprocessor (µP)) performs the switching events necessary in its function. The capacitor to act as a local source of charge that provides enough current to the switching elements. If decoupling is inadequate, the IC may experience voltage droop or signal pulse spiking or the like, which may result erroneous detection of the IC’s logic elements.

Decoupling is typically achieved at several levels in the power design of an electronic system, each higher level “cascading” to a lower level of decoupling. With the cascaded decoupling scheme the capacitance required is usually reduced with the decoupling levels closest to the IC. The maximum allowable inductance (ESL) for the decoupling capacitors used also typically decreases as the proximity of the IC is approached. Multilayer ceramic capacitors (MLCC) are most suitable for decoupling on the IC package as MLCC offer a unique combination of low ESL, high capacitance density, small package size and low ESR (equivalent series resistance) for these typically low voltage (<-5V) applications. Design for optimal decoupling is well described in the literature.¹,²,³
Over time, developers have been able to develop the design of the basic MLCC in order to reduce the ESL of the MLCC without significantly reducing capacitance per unit volume. Designs such as reverse termination MLCC, interdigitated capacitors, low inductance array capacitors, and the like have served to enable IC decoupling at increasing frequency and with reduced switching voltages. These designs, while useful, have been less than ideal. Some designs require buried via circuit patterns which are relative expensive and typically add parasitic inductances to the circuit that may exceed the ESL of the capacitor, while other designs may not have inductance values that are low enough to be suitable for the application, etc.

**Discussion**

KEMET's D-Stick™ and D-Pack devices offer a paradigm change in decoupling capacitor design. D-Stick™ devices are designed for high capacitance density combined with low inductance. Additionally D-Stick™ has the benefit of “straight through” electrode design providing a path for power to and from the microprocessor as illustrated in Fig. 1. Because of this, D-Sticks are used for both power delivery and for decoupling. This allows for space savings in the IC package as the I/O pins or balls are replaced with D-Sticks, eliminating the need for on package decoupling MLCC. Additionally the design is excellent for power noise filtering and provides a thermal path from the bottom side of the IC package as well as an electrical path. The dimensions physical may be modified as well as the pitch of the I/Os and the number of I/Os on the device. The D-Stick™ design is modular in that it can be combined in various configurations. Since the D-Stick becomes part of the power and ground connections, there is no additional circuitry required to connect the capacitance to these connections, thereby eliminating the parasitics of these appendage circuits.

![Diagram of D-Stick](image)

**Figure 1. D-Stick™**
KEMET’s D-Pack takes D-Stick™ to the next level. D-Stick™ elements are combined together into an array designed to match the power I/O structure of the IC package as illustrated in Fig. 2. Partial interposer D-Packs are comprised of D-Sticks only, while full interposer D-Packs also include signal I/Os. The full interposer D-Pack offers the further advantage of one placement/alignment and reflow operation which reduces the complexity of IC package assembly and attach. The final interposer assembly is illustrated in Fig. 3. In this example, the assembly requires no increase in the X or Y dimension over a standard package with I/O population of the full bottom surface. The height of the interposer is ~1.25 mm which is only a slight addition to the height of BGA balls (0.6mm) or a slight reduction in height in the case of 2 mm PGA pins.

Figure 2. D-Packs

Figure 3. Assembled IC package to circuit board, with D-Pack as interposer
D-Pack offers excellent capacitance density. D-Packs are available with aerial capacitance densities of \(~1,000 \mu F/in^2 (\sim 150 \mu F/cm^2)\) for devices meeting X5R/X6S/X7T ratings. Capacitance densities under typical use conditions (ca. 85-105C, 1 VDC bias, 0.1VAC) can be as high as \(~690 \mu F/in^2 (\sim 100 \mu F/cm^2)\) as indicated in Table 1. A 100 unit D-Pack has very low ESL and ESR combined very high insertion loss. This D-Pack also have very low through pin resistance, leading to loss of less than \(~1\%\) of power (RT value) when operated at \(~200A\).

Table 1. D-Pack properties for 100 D-Stick™ D-Pack

<table>
<thead>
<tr>
<th>Property</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capcitance (RT, 1VAC, 1KHz), (\mu F)</td>
<td>620</td>
</tr>
<tr>
<td>Capacitance Tolerance, %</td>
<td>K (+/-10%) M (+/-20%)</td>
</tr>
<tr>
<td>Capacitance at 105C, 1VDC, 0.1 VAC 20Hz</td>
<td>430</td>
</tr>
<tr>
<td>ESL (@ MHz), (\mu H)</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>0.93</td>
</tr>
<tr>
<td>100</td>
<td>0.85</td>
</tr>
<tr>
<td>1000</td>
<td>0.59</td>
</tr>
<tr>
<td>ESR (@ MHz), (\mu Ohm)</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>31</td>
</tr>
<tr>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>100</td>
<td>145</td>
</tr>
<tr>
<td>1000</td>
<td>2500</td>
</tr>
<tr>
<td>Through Resistance (DC), (\mu Ohm)</td>
<td>&lt;40</td>
</tr>
<tr>
<td>Insertion Loss (@ MHz), dB</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>97.5</td>
</tr>
<tr>
<td>10</td>
<td>108.5</td>
</tr>
<tr>
<td>100</td>
<td>89.0</td>
</tr>
<tr>
<td>1000</td>
<td>70.0</td>
</tr>
<tr>
<td>Current carrying Capability (A) @105C, &lt;25C Delta T*</td>
<td>210</td>
</tr>
<tr>
<td>Power dissipation (RT), %</td>
<td>&lt;1 (~0.85%)</td>
</tr>
<tr>
<td>Pinout Pitch, mm</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>1.0</td>
</tr>
<tr>
<td>Y</td>
<td>1.0</td>
</tr>
<tr>
<td>Height (Z), mm</td>
<td>1.15</td>
</tr>
</tbody>
</table>

*Solder, interconnects and board included

Since the D-Pack is not mounted on the top side of the IC package, the package circuitry can also be simplified as package layers dedicated to decoupling to top side decoupling capacitors may be eliminated. Additionally, used as an interposer, D-Pack does not suffer from other difficulties associated with the use of topside decoupling capacitors such as height restrictions, lid attach issues, heat sinking issues or the like as indicated in Fig. 4. D-Pack does not require expansion of the aerial size of the IC package as does bottom side decoupling (see Fig. 5).
Figure 4. Limitations of top side decoupling

- Requires additional decoupling layers in package (cost)
- Exhibits relatively high level of loop inductance (a vs. b)
- MLCC chip dimension limited by IC height/thickness
- MLCC may interfere with lid attach
- MLCC may interfere with heat sinking scheme

Figure 5. Limitations of bottom side decoupling

- Requires additional package size
- Reduced thermal cycle performance
- Reduced bottom-side heat flux per unit area
- Increased power/ground trace lengths
- Increased package costs
The D-Pack configuration is designed to replace all power and ground I/Os to the µP package. The pitch of the terminals on the D-Pack matches the pitch on the µP package, as well as the pitch on the PCB motherboard. The thickness of the D-Pack (~0.8 to 1.5 mm with 1.15 mm for the design illustrated) is designed to work with pin grid array (PGA) packaging as a partial interposer, or with ball grid array (BGA) or land grid array (LGA) packaging as a full interposer as illustrated in Fig. 2. The planarity of the D-Pack is controlled in order to ensure excellent mechanical and electrical connection between the motherboard PCB and the µP package.

The D-Pack design can be specially configured to the needs of the customer/µP package designer. The pitch of the D-Pack is typically 1 mm (X and Y directions), but can be adjusted from ~0.5 mm to ~1.5 mm as needed. The IC package design does need meet the requirements of the modular capability of the individual D-Stick™ design however. This may require modifications in IC package design. An ideal IC package pin out is shown in Fig. 6. In this ideal design, all power and ground are routed in a “checkerboard” pattern through the center of the package. The signal I/Os are placed in a “window frame” periphery around the power and ground core in the center of the package. Modifications on this pin out structure are possible, but some pin out structures (e.g., signal I/O interspersed with Power and Ground I/O over the entire structure or the like) are not easily accommodated using D-Pack.

Figure 6. Example of a generic ideal package IC pin out for D-Pack
The overall capacitance of a D-Pack is additive from the D-Sticks. For example, a 100 D-Stick D-Pack made with 100 each of 5 µF D-Sticks will have a net capacitance of ~500 µF. The amount of capacitance in a D-Pack can be varied by D-Stick design as well, ranging from ~1 µF to ~7 µF within a D-Stick, or from ~100 µF to ~700 µF, or as high as ~175 µF per cm² (~1,130 µF/in²) board space (which would otherwise be used for power I/O) for the 100 D-Stick D-Pack example described above. Depending upon the design situation, this amount of capacitance in near vicinity to the µP may enable reduction or elimination of higher level decoupling capacitors as well, resulting in further space saving on the motherboard as well as significant cost reduction through elimination of, now unnecessary decoupling capacitor components.

For the above sample, the total number of I/Os is 400 (200 power I/Os and 200 ground I/Os). Each I/O is designed to accommodate ~1 ampere with minimal ΔT. The through pin resistance of each I/O is on the order of 6 to 8 mΩ, which is less than the through pin resistance of a 2 mm PGA pin LGA mounted.

The capacitance and inductance properties of a D-Pack may be estimated using a simple parallel circuit analogy, the overall inductance of a D-Pack may be estimated by the number of D-Sticks within a D-Pack through the relation:

\[
L_{D-Pack} \approx \frac{L_{D-Stick}}{N_{D-Stick}}
\]

where:
- \( L_{D-Pack} \) is the inductance of the D-Pack
- \( L_{D-Stick} \) is the inductance of each of the component D-Sticks
- \( N_{D-Stick} \) is the number of D-Sticks within a D-Pack (note: assumes all D-Stick™ terminals are mounted as in application for inductance measurement)

The overall through pin resistance of the D-Pack may be estimated through the relation:

\[
R_{D-Pack} \approx \frac{R_{D-Stick}}{N_{D-Stick} \times \left( \frac{n_{I/O per Stick}}{2} \right)}
\]

where:
- \( R_{D-Pack} \) is the through pin resistance of the D-Pack
- \( R_{D-Stick} \) is the through pin resistance from 1 power to 1 ground terminal of each of the component D-Sticks
- \( N_{D-Stick} \) is the number of D-Sticks within a D-Pack
- \( n_{I/O per Stick} \) is the number of I/O pairs per D-Stick (note: this number is divided by 2 for power and ground). Note: If resistance of all power or ground terminals is measured for the D-Stick™ at one time, \( n = 2 \)

Similarly, the overall impedance from power to ground may be estimated through the relation:

\[
Z_{D-Pack P to G} \approx \frac{Z_{D-Stick P1 to G1}}{N_{D-Stick} \times \left( \frac{n_{I/O per Stick}}{2} \right)}
\]
where:

\[ Z_{D-Pack} \] is the impedance of the D-Pack from power to ground

\[ Z_{D-Stick} \] is the impedance of each D-Stick™ from 1 power terminal to 1 ground terminal of each of the component D-Sticks

\[ N_{D-Stick} \] is the number of D-Sticks within a D-Pack

\[ n_{I/O \ per \ Stick} \] is the number of I/O pairs per D-Stick (note: this number is divided by 2 for power and ground). If impedance of all power to all ground terminals is measured for the D-Stick™ at one time, \( n = 2 \)

As mentioned above, the D-Pack also serves as an effective C-type power filter, which is an added benefit of the D-Pack interposer configuration. The overall insertion loss of the D-Pack may be estimated from the insertion loss (IL) of the component D-Stick™, through the relation:

\[
IL_{D-Pack} \approx IL_{D-Stick} + 20 \log_{10} \left( \xi \cdot N_{D-Stick} \right)
\]

where:

\[ IL_{D-Pack} \] is the insertion loss of the D-Pack in dB

\[ IL_{D-Stick} \] is the insertion loss of the component D-Stick™ as determined through the relation:

\[
IL_{D-Stick} = 20 \log_{10} \left[ \frac{Z_{D-Stick}}{25 + Z_{D-Stick}} \right]
\]

where:

\[ Z_{D-Stick} \] is the impedance of the D-Stick at the frequency of interest when using a vector network analyzer (VNA) with 2 port shunted configuration as described below and where:

\[
Z_{D-Stick} \approx -25 \cdot S_{21D-Stick}
\]

where:

\[ S_{21D-Stick} \] is the \( S_{21} \) value of the D-Stick measured as described below

\( \xi \) is the number of power and ground I/O pairs per D-Stick (note that if all power and ground I/O pairs were connected during the IL measurement, \( \xi = 1 \))

These relationships have been verified through a detailed and proprietary analysis of 76 D-Stick™ unit D-Packs mounted to a µP packages, tested using a VNA and modeled using proprietary modeling methods. The results of this study agree well with the individual D-Stick™ data discussed below when using the above equations.

In order to understand the electronic properties of D-Pack, it is imperative to understand the properties of the D-Stick™ components. D-Sticks may be made with any suitable dielectric material. Since maximum capacitance per unit volume or volumetric efficiency (VE) is typically desired for a decoupling application, the dielectric used for development for D-Pack applications is a thin layer, high K, class 2 BME dielectric materials set suitable for X5R, X6S or X7T application as indicated in Fig. 7. Voltage ratings are set specifically for the customer’s application via D-Stick™ design and use of a FITs (failures in time) relationship modified to more accurately predict LIFE performance using the PV (Propokowicz-Vaskas) relation. These projections are derived from and correlated to extensive HALT (highly accelerated life test) and LIFE test data.
The impedance of D-Stick™ devices from power to ground has been measured in numerous ways, all with reasonable agreement. This is true for the insertion loss of D-Stick™ devices as well. Perhaps the best way to characterize D-Sticks for these values is to use a VNA with custom designed fixturing. Fig. 8 illustrates the VNA probing set-up used to make the D-Stick impedance and insertion loss measurements. Measurements were made with vertical internal electrode orientation solder mounting to the fixture with bottom terminals only as illustrated in Fig. 9. $S_{21}$ data were captured using an Agilent 8753ES VNA through 40A-GS-300-P microprobes from 300 KHz to 6 GHz, and converted to impedance data after SOLT (short-open-load-through) calibration using a CS14 calibration substrate. The reference plane of the DUT (device under test) was set at the probe boundaries and a short fixture was utilized to establish the impedance of the fixturing, which was removed from the calculated impedance data of the DUT, in order to yield the D-Stick only data.

The resulting insertion loss data are illustrated in Fig. 10, while the impedance, equivalent series inductance (ESL) and equivalent series resistance (ESR) data are illustrated in figures 11, 12 and 13 respectively (each plot is an average of 11 pieces for all measurements). Insertion loss for D-Sticks indicates that the D-Stick™ is a nearly ideal electronic filter, with characteristic slope of ~20dB/decade frequency and very low onset frequency. As noted above, a 100 D-Stick™ unit D-Pack should exhibit an increase in insertion loss of ~40dB over a single D-Stick™, approaching the practical maximum for a filter of ~120 dB as projected in Fig. 16. The measured inductance of D-Sticks is quite low (<100 pH). These data agree well with 76 unit D-Pack measurements that indicated the inductance to be ~1 pH using a proprietary methodology.

D-Stick™ devices having other different configurations with respect to case size and I/O counts are also available. D-Stick™ devices with 8 pairs of terminals (4 power and 4 ground terminals on each side) in the 0516 case size have been demonstrated exhibiting ESL values in the 30 pH range as well. These devices have a design capacitance of 10 µF and should be an excellent candidate for either on µP package decoupling as is currently used or as an interposer device.
Figure 8. VNA probe set up for impedance and insertion loss measurements of individual D-Sticks

![Image of VNA probe setup]

Figure 9. Device configuration

\[ Z_{dutS21} = \frac{-25 \times duts21s1}{duts21s1 - 1} \]
Figure 10. Insertion loss data for D-Stick™

Figure 11. Impedance data for D-Stick™
Figure 12. Inductance data for D-Stick™

Figure 13. Power to ground equivalent resistance for D-Stick™
Figure 14. Projected insertion loss for D-Pack

Figure 15. Inductance of 16 Terminal D-Stick™
D-Pack devices have also proven to perform well in thermal cycle testing. Partial interposer D-Pack performance when solder mounted using either SAC 305 or Pb/Sn solder is indicated in Fig. 16. The data indicate that either solder system should provide \(<\sim 1\%\) failure rate with \(\sim 1000\) or more thermal cycles. Full interposers are on test and have also exhibited promising results (1000 cycles to failure) to date with a 2” x 2” (5 cm x 5 cm) package configuration.

![Probability Plot of SAC CTF, Pb/Sn CTF](image)

Figure 16. Thermal cycle performance of partial interposer of 100 unit D-Pack mounted between LTCC ceramic package and multilayer FR4 board with SAC 305 (ΔCTE \(\sim 7\) ppm/°C, 10 min/10 min/10 min/10 min cycle, 0 to 100°C)

D-Pack devices are designed to handle high current density. Fig. 17 illustrates the rise in temperature of a 100 unit D-Pack in an ambient of 105°C after at least 30 minutes exposure to the current density indicated. D-Pack current density capability is suitable for \(~1\) A/pin with ΔT \(<20°C\) at 105°C ambient or slightly more than 100 A/cm² assuming maximum allowable ΔT of 25°C.
Summary and Conclusion

Decoupling needs have evolved over time. Needs for reduction in ESL, combined with maximization of VE have been important drivers for development of solutions to meet high speed decoupling needs of customers. D-Pack, a new interposer decoupling solution is a very effective decoupling solution, having very high capacitance (ca. 1,000 µF/in²) in very close proximity to the µP package and with extremely low inductance (ca. 1 pH) without requiring an increase in µP footprint. The D-Pack configuration has very low combined through pin resistance, robbing little power from the µP (~1% or less for a 100 D-Stick™ unit D-Pack and 250W µP operating at 1V). D-Pack does not hinder thermal management and enables minimal aerial IC package dimension which allows for improved thermal cycle performance as well as reduced package cost. D-Pack has exhibited excellent thermal cycle performance. D-Pack can handle very high current densities (in excess of 650 A/in² (>100 A/cm²)). Additionally, D-Pack provides excellent power noise filtering with insertion loss nearing 120 dB.

2  www.seattlerobotics.org/encoder/jun97/basics.html
6  “Multilayer Ceramic EMI Filters,” Syfer Technology, Ltd.