Surge Step Stress Testing (SSST) of Tantalum Capacitors

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Abstract

A misunderstanding of the failure mechanism of tantalum capacitors has created the fear of using these capacitors in high current applications. A capacitor depends on the dielectric as an insulative material and the plates as a conductive material. If the current was the trigger mechanism for failure, then the plates should be suspect throughout the life of the capacitor. This is not the case as the failures with this capacitor are normally related to initial power-on occurrences. As such, the failure mechanism is most likely the breakdown of the dielectric when exposed to a specific critical strain for the first time. The high available current ensures that the failure does not heal itself, but breaks down the dielectric so catastrophically that the dielectric loses most of its insulative properties. This Surge Step Stress Test (SSST) is intended to identify the critical stress level of any batch of capacitors to give some predictability to the power-on failure mechanism.

Surge Current Failure Reputation

Tantalum capacitors have a reputation whereby a great deal of concern is focused on the inrush current magnitude. We have been repeatedly exposed to catastrophic failures in circuits where the current is unlimited and the device fails short and then continues to generate extreme heat as current continues into the fault. The exposure to this failure has led us to recommend that the device have some series resistance as a current limiting function, eliminating almost all of these types of experiences. We associate the failure with high current and we define the fault development as related to current; but we have only identified a secondary characteristic of these failures.

The test that was used to support this theory consisted of power-on voltage applications to samples of capacitors using various resistor values to limit the peak current. Because the higher values of series resistance created fewer failures, the conclusion was that the magnitude of the current created the differentiating point of failures.

The fault avalanche, or collapse, is not due to the current, but is related to the voltage stress on the dielectric. The capacitor's dielectric is an insulator, and when it fails, it reverts to its opposite characteristic, becoming conductive. The higher current does not create the defect, but is a secondary catalyst that pushes the dielectric breakdown into an ignition mode, rather than allowing a self-healing to occur. The failure is not the result of a poor conductive path in charging the plates; but it is the insulative dielectric, which breaks down and collapses. Its primary activation is voltage stress, not localized current constriction. Eliminating the current does not eliminate all failures. It only alters the method of presentation of these failures to the outside observer.

Yet adding series resistance to the circuit does seem to eliminate the number of reported tantalum failures. The failure totals noted in a circuit with significant resistance can appear to support the claim that the failures are not only less catastrophic in higher resistance circuits, but the numbers of reported failures can be found to be significantly lower. What else can be going on with this device that refutes this evidence against current limitation?

MnO_2 and Self-healing

The cathode plate structure in a tantalum capacitor is created with the formation of manganese dioxide ($MnO_{2)}$

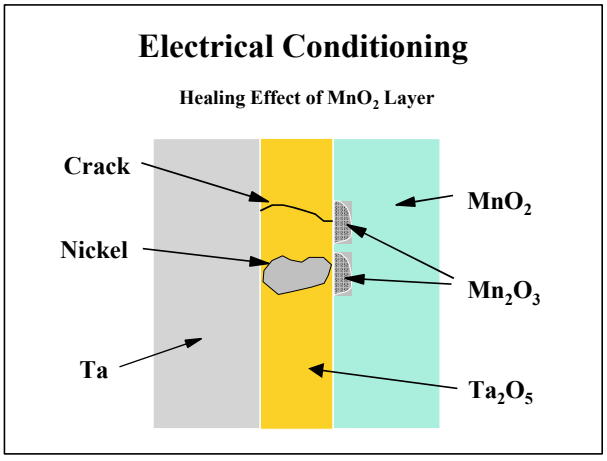

Fig. 1. Self-healing or aging process of solid tantalum.

along the surface of the tantalum pentoxide dielectric, which was formed along the surface of the exposed tantalum [1]. The use of MnO_2 allowed the tantalum capacitor to advance from a wet slug capacitor to a solid-state device. In a wet slug capacitor, the electrolyte is treated to allow a refresh of the anodization on the surface of the valve metal. Refreshing aluminum capacitors after long periods of shelf storage rebuilds the dielectric in this manner. However, MnO_2 was employed not because of its ability to mimic this characteristic, but because it can shut down current into a fault site. This self-healing mechanism creates converted areas of the MnO_2 to act as *caps* at the leakage sites as shown in Fig. 1.

The current in a small defect within the dielectric is concentrated at the point of egress into a small, finite volume of the cathode plate in contact with the fault site. This concentrated current causes the temperature within this very small region to rise significantly. As the MnO_2 heats up past 380°C, it begins to release oxygen, changing the material structure from MnO_2 to a reduced state such as Mn_2O_3. Because this reduced material has much higher resistivity than the original, the current going through this fault is pinched off. This effect is called self-healing because it eliminates the fault site from the active electrification of the capacitor, though it has not healed the fault site at all [2].

The heating of the MnO_2, the release of oxygen, and subsequent conversion to the reduced state does not take place immediately. Some small but finite time is required for this process to complete itself. Here's where the current magnitude is critical. If the circuit current is unrestricted, then there is no restriction of current into the fault site. The MnO_2 starts to convert and release oxygen, but the current continues to rise in the dielectric. The Ta_2O_5 dielectric converts from its insulative, amorphous state to a conductive crystalline state at ~480°C. As a site draws more current, it converts adjacent sites to crystalline states, growing radially outward. It spreads the current to a wider area of MnO_2, thereby reducing the current conversion. The heat spreads into the tantalum base metal, and in this elevated temperature state, the tantalum rapidly absorbs the released oxygen. More heat is generated and more MnO_2 is converted by conducted thermal radiation from the fault site. This chain reaction soon envelops a very large volume of the pellet structure of the tantalum capacitor, with tantalum rapidly oxidizing and generating enormous heat.

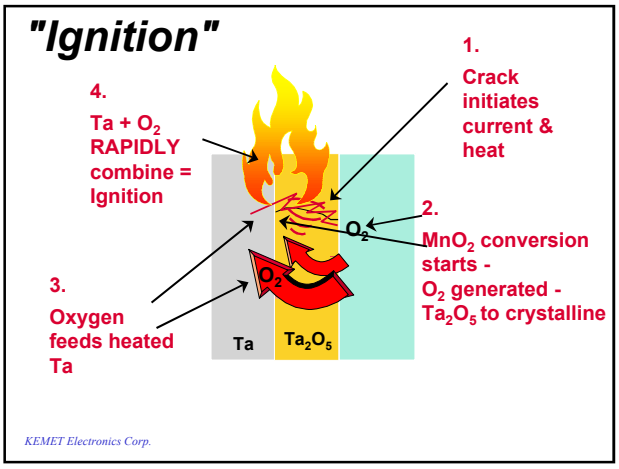

Fig. 2. Ignition failure mode with unrestricted current.

Remember that the initial fault mechanism is the voltage collapsing within the dielectric. Secondary issues of the rapid oxidation are initiated by the energy delivered into the system. With the higher CV product being developed today, we now have self-contained energy within the capacitor that is high enough to trigger this secondary reaction without a high external current being supplied.

SSST - *Surge Step Stress Test*

What we are attempting to do with this test is to establish a stress level at which each capacitor ignites under a high current application. We believe that the stress level or voltage across the dielectric is the trigger mechanism for the breakdown, and that the current pushes this collapse into a catastrophic failure. In order to establish the stress level for each capacitor, it is subjected to voltage pulses of increasing magnitude from a low impedance source.

This test is a variation of a "Step Stress Life Test" that was presented to us by Bell Laboratories [3]. In this test, they incremented the voltage in timed steps as the part was under elevated temperatures. Jim Marshall of KEMET directed conversion of the "Step Stress Life" to the SSST test. The conversion put more emphasis on the voltage magnitude, and less emphasis on pulse duration.

The capacitors are mounted to a circuit board (FR-4) using an IR-reflow solder process. The boards pass through

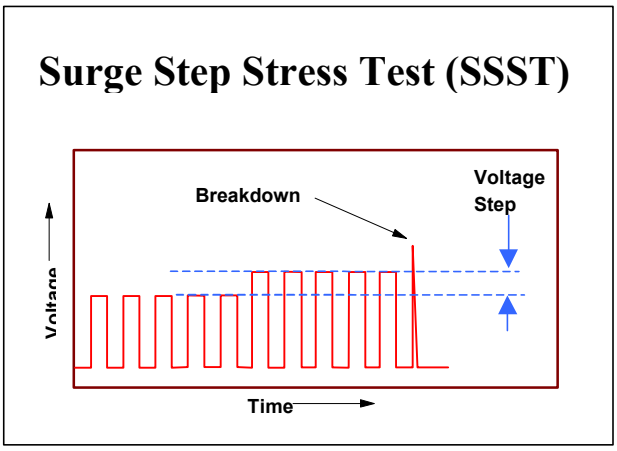

Fig. 3. Increasing voltage pulses of SSST test.

the IR chamber for two passes to exercise the latent forces developed in the manufacturing process in an attempt to generate deviations in performance [4]. We use a twenty piece board skipping alternate positions (10 per board) to prevent false failures due to damage from adjacent burning units.

The capacitor is charged to the set voltage, held at that voltage for ½ second, and then discharged through a dead short for ½ second. This sequence is repeated five times. After the fifth pulse, the voltage setting is incremented slightly, and the next pulse train applies the higher voltage pulses to the capacitor. This five-pulse cycle is repeated at incrementally higher voltage until the capacitor breaks down. When we monitored which pulse the failure occurs on, we no pieces failed on secondary pulses, as the initial pulse triggered the dielectric collapse with an elevated stress level.

The voltage for the first pulse train is set to ½ of the rated voltage. The final voltage is at 4x of the rated voltage. The step voltage is based on the range from start to stop, to allow a full test to take place within a 15 to 40 step sequence. Step increments of 0.1, 0.5, 1, 2.5 or 5 VDC are selected based on the starting voltage and the range.

The power supply is high current, capable of supplying tens of amperes at a constant rate. The input to each capacitor is isolated and buffered with a 12,000-uF-capacitor bank to assure high charge currents. Three parallel FETs switch on the current to the individual capacitor, each with a turn-on resistance of less than 20 milliohms. The discharge of the test capacitor is again through three parallel FETs, into a dead short. Total circuit resistance in the charge and discharge modes is approximately 0.3 ohms.

The pass-fail criterion is a voltage measurement across the capacitor, just prior to discharge. If the voltage is within 95% of the set voltage, the unit is deemed to have passed. Once any test position fails, the voltage level at which it fails is recorded. Testing is completed when all the pieces have failed, or the maximum set voltage of 4x rated voltage is achieved. The allowable 5% differential between set and measured voltage prevents false failure indications from high leakage units.

Weibull Analysis

The failures as reported to us by our customers become an issue when they become sensitive to the failure rates reported, or when safety concerns are confronted. In either of these cases, the unacceptable failure rate can range anywhere from 100 PPM to thousands of PPM. Depending on the actual failure rate detected, an extremely large sample, equivalent to several manufacturing batches, would be required to have the sensitivity in our testing that would give us the resolution of their reported failures. From a practical aspect, we needed a combination of 1), a more reasonable sample size and 2), predictive statistical methods to evaluate or extrapolate a failure rate distribution lesser than the percentage resolution of the sample. Weibull analysis became the tool of choice. [5,6]

Fig. 4 is a Weibull plot of SSST data. Failure voltage is represented on the horizontal scale, and cumulative percent failed is represented on the vertical axis. The failure results are represented as dots, with a best-fit linear regression line calculated and drawn through them. A few more procedural details follow.

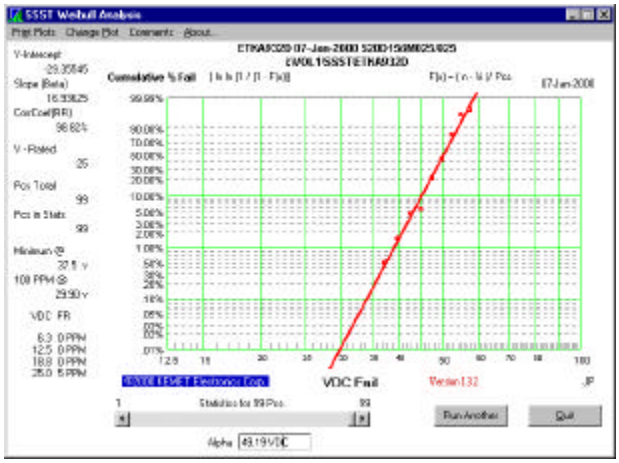

Fig. 4. Weibull plot of SSST data.

The application of voltage to the samples is not continuously rising, but is step incremented. We expect that at each voltage setting, a number of capacitors will fail. Accordingly, the data is grouped by increasing voltage, and only one point, representing the total cumulative percent failed, is plotted at each voltage level.

In this example, 99 pieces were tested and all 99 pieces were used in creating the *fit*. Because multiple failures are recorded at most voltage increments, these 99 pieces are relegated to only 9 data points in the plot.

The sample size of 99 pieces represents results on a submission of possibly 100 pieces. This discrepancy (100 versus 99) recognizes that the system has two potential measurement shortcomings. First, because we measure the voltage on each pulse just prior to discharge, there can be an instance in which the unit breaks down and ignites with enough violence to be thrown from the board, resulting in an open condition. In the ½ second of the pulse duration, this sequence can occur with the final measurement resulting in a "no fail" indication. We believe that at the final voltage of 4x rated, all the devices should have failed, and any of the total submitted samples that do not register with some failure level are discarded as non-existing pieces of the sample. The 100 pieces tested, with only 99 registered readings, is then relegated to calculations for a sample size of 99 pieces.

The second potential shortcoming involves the debris created within the test enclosure. We attempt to keep the fixture clean for good contact, but the violence of many of these failures (especially close to 4x rated as the energy is equal to $\frac{1}{2}CV^2$) creates burns, charring, and carbon deposits along the contact assembly. We have measured units that have no indication of failure as parametrically good after 4x exposure, and we believe that poor contact or "open" conditions prevented application of the voltage.

Additionally, FETs fail periodically, and the associated channel will report failures at initial application levels, consistently from test group to test group. The operator can select to have this channel omitted for all the test data generated.

Returning to the plot of Fig. 4, the pieces are rated at 25 VDC, and the lowest failure occurs at 37.5 VDC. In itself, this minimum value might indicate that the lowest failure voltage for the population would be near this, but extending the *fit* to lower percentages, the 100-PPM level is estimated to be at 29.9 VDC. As this level is still greater than the rated voltage of the samples, these results are relatively good. The *Y-Intercept* and *Slope* for the fitted line are given to the left of the plot. The slope is the *Beta* (shape) parameter of the Weibull plot. *Alpha* (characteristic life) is also shown at the extreme bottom of the display. Finally, the correlation coefficient squared or "*RR*" is given as a percentage.

All of the data points in Fig. 4 are included in the *fit* as they all show a close approximate grouping along the line. The plot defaults to either the first 8 voltage increments, or in the case where grouping the data points to common levels results in fewer then 8 points, all of the points would be included. However, the operator can use the horizontal scroll bar at the bottom of the plot to define the data points to be included. This election is made whenever the data do not fit well, and analysis is enhanced by excluding points at the higher voltage increments as in Fig. 5 (which are not as important as those lower and nearer to the voltage stress levels of the application). This is a subjective judgement on part of the operator, and variations among operators should be expected. Additional examples shown later will cover bi-modal effects, which appear in many of the sample plots.

Bi-modal Distributions

Using the standard voltage levels of 25%, 50%, 75%, and 100% of rated voltage, the projected failure rates in Fig. 4 are 0, 0, 0, and 5 PPM, respectively. Let us point out that 5 PPM at rated voltage is exceptionally good. A more typical response is depicted in Fig. 5. Here is a 16 VDC part with a projected 100 PPM failure rate at 9.34

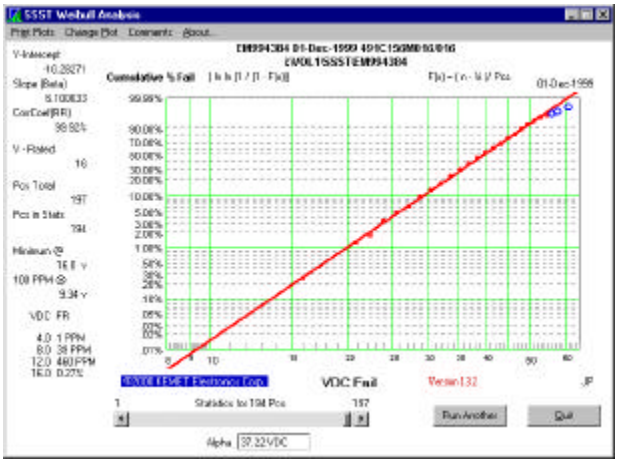

Fig. 5. Plot showing slight bi-modal effect.

VDC (58% of rated). The failure rates at the standard voltage levels of 25%, 50%, 75%, and 100% are 1 PPM, 39 PPM, 460 PPM, and 0.27%, respectively. These results reemphasize manufacturers' recommendations for derating to 50% of rated voltage.

The 26 points on this plot represent the 26 discrete voltage levels at which failures were recorded. Only 23 out of the 26 were included in the *fit* because the last three appear to deviate or trend away from the initial grouping. Since these 23 points represent 194 ("Pcs in Stats") out of 197 pieces ("Pcs Total"), we can easily see that these three *odd* points represent one individual piece, each. The exclusion of these points enhances the *fit* and consequently the accuracy of the failure rate estimate in the voltage range of interest.

Fig. 6 depicts another set of bi-modal results in which the first 15 points, representing 46 pieces, are selected to generate the *fitted* linear interpolation. The remaining 12 points represent the remaining 140 pieces of the sample. In this case, a major portion of the sample data is excluded to enhance the accuracy of predictions in the primary area of interest. . We believe that the effects of the IR reflow can create deviations from the main failure distribution, sometimes affecting only a portion of the sample. Here in Fig. 6, this portion that we believe to be effected represents only about 25% of the sample.

By extrapolating the *fit,* we can estimate the predefined voltage level failure rates of 6 PPM, 136 PPM, 814 PPM, and 0.29%. If this chip is being used in an application above the 50% rated voltage level, the failure rate could be a problem; if used below this level, the failure rate may not have even been noted. The projected 100-PPM failure rate level is shown to be at 7.47 volts, close to the 50% (8.0 VDC) rated voltage level. As such, this again points out that use of this device at 50% rated voltage or less, would not result in a noteworthy number of failures.

So far, the bi-modal examples presented appear to be influenced by the forces in the solder process, creating apparent excursions below previous screening limits. Due to these excursions, it is not unusual to find a piece failing slightly below this screened limit, even in relatively small sample sizes between 80 and 200 pieces.

Fig. 7 is indicative of a truncated distribution possibly created by doing 100% production screening of this

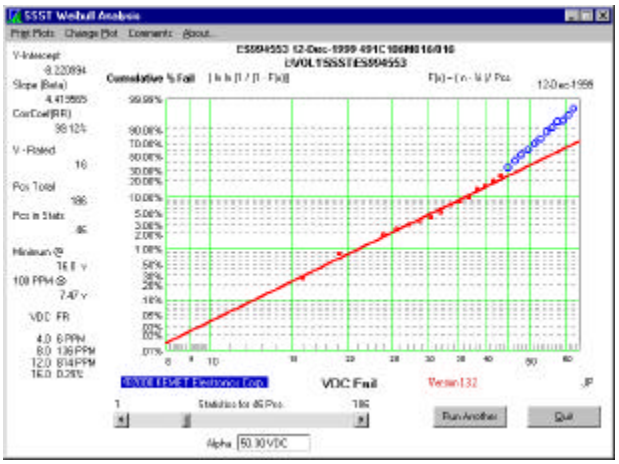

Fig. 6. Greater bi-modal effect splitting data.

group at 10 VDC. As the distribution nears the screened 10 VDC limit, it appears to be skewed downward. If the sorted limit were to remain intact (no disturbance of the distribution after screening), then a large enough sample would reveal a true failure rate very close to 0 PPM at 10 VDC. Logically, there would be no failures below 10VDC, and the slope of the lower part of the failure rate distribution would approach infinity.

Sample Preparation – Critical Factors

The solder reflow conditions are critical to the severity of the forces developed within the component during mounting, and have a direct relationship on the results of this test. In some cases, this test has shown remarkable correlation to production data (PPM failures vs. projections), and at other times, the correlation is weak. Water wash can exacerbate ionic penetration into the package (plastic does not create a hermetically sealed package). In

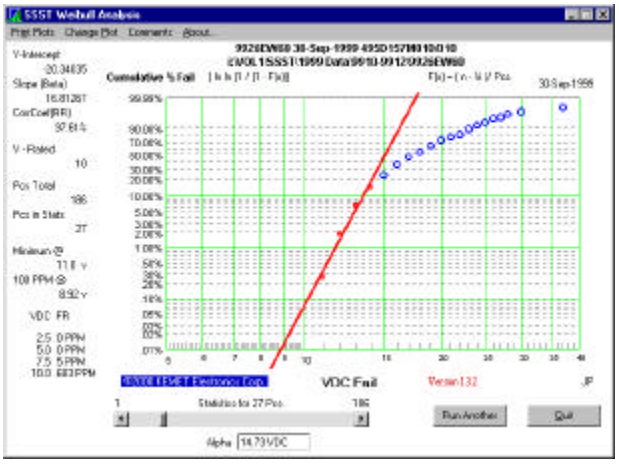

Fig. 7. Truncating bi-modal effect.

short, there are many factors that can influence actual results to differ from projections, including the subjectivity of the selection of data points for the *fit*.

Default Conditions

KEMET's SSST software allows the operator to change certain default conditions or calculations (Fig. 8). Earlier we mentioned that the vertical axis of the Weibull plot represents the cumulative percent failed. More precisely stated, the vertical plot positions are determined by an *adjusted percentile of failure* calculation. Two methods are provided to create this adjustment. Many prefer the "$(\Sigma_i\text{-}.5)/n$" method, in which "Σ_i" represents the "i^{th}" cumulative failure summation, and "n" represents the total sample size. The second choice provided is the familiar "$\Sigma_i /(n+1)$" calculation, in which the total count is incremented by one.

We also mentioned earlier that only one point is plotted at each voltage increment, representing all the cumulative failures in that increment added to the cumulative failure point in the previous increment. In fact there is an option to plot *each* failure and then use all the points in the *fit.* This method may provide additional confidence in the *fitted* line as the degrees of freedom increase with the additional points (within KEMET there are varying opinions regarding which method is preferable).

The appearance of the "grid lines" can also be determined here. The vertical and horizontal axes each have major and minor divisions that can be presented as lines or simply as tics. The x-axis range can be varied from ½ rated voltage up to 4x rated voltage (preferred), or from ½ rated voltage to the next decade beyond the 4x rated voltage level. The default data file location (*drive* and *path*) can be changed from here. Additionally, the default number of data points used to generate the initial *fit* can be changed here (default is 8).

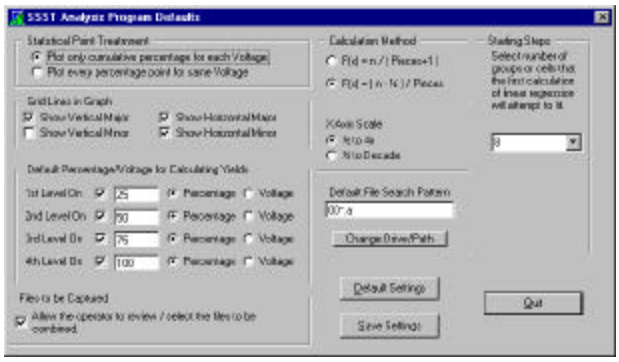

Fig. 8. Default settings of analysis software.

Correlation to "Real World" Applications

This test creates or uncovers failures, generating "variables" type data to reflect sensitivity to given stress levels. Because the stress is applied incrementally until failure, the question arises as to whether the earlier steps (lower voltages) "condition" the parts, making them less susceptible to failure in later steps. If this effect were present, the test results would err toward lower failure rates, since under actual use those parts would not have the "benefit" of "conditioning" at incremented voltage stress. Even though minor flaws may heal at lower stress levels, we believe that application of this breakdown level without the earlier steps would lead to equivalent results. We believe that minor flaws will self-heal, regardless of these conditions.

This belief rests primarily in the logic that the available high inrush current allows little time for the self-healing mechanism to take place for the major faults with higher currents. The minor faults have higher resistivity, lower currents: thus allow some time delay for activation of the self-healing. (We have an additional test that utilizes a lower constant current and fully variable voltage increases, that can be found in "*Update – Scintillation Testing of Tantalum Capacitors*".)

Within our production sequence, parts are exposed to 100% of rated voltage, and slightly higher, at several points within the process. For DC leakage and "surge *voltage*" testing, each part is brought up to voltage through some series resistance. It is only during "surge *current*" screening that parts are exposed to test voltage through extremely low resistance circuits (as the SSST tester is configured). Power supply application devices (T495 and T5xx) are screened in this high current environment to 100% of rated voltage. Commercial devices are normally screened at 75% of rated. Only in this "surge *current*" screening can we be assured that full test voltage is applied to the part. All other "resistance limited" screens are subject to "scintillations" that prevent the capacitor from achieving full test voltage. This screening may truncate the inherent failure distribution as shown in Fig. 9; but, because of the forces

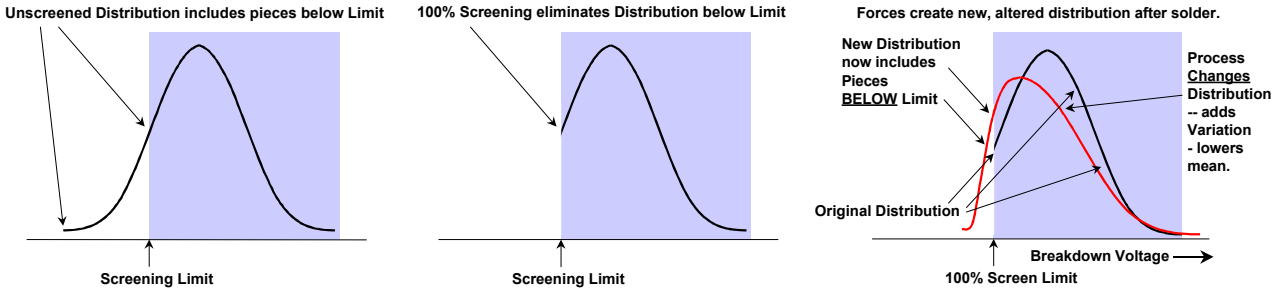

Fig. 9. Screened limit truncates distribution, but distribution may change after exposure to solder process.

created on the part during the solder process, new fault sites can be created. The distribution can include voltage levels that will fail located below the screened voltage level

Conclusion

We have described some of the developmental philosophy, operational details, highlights and limitations of KEMET's Surge Step Stress Test. Certainly, those limitations may contribute to some inconsistent correlation between SSST projections and actual failure rates. Again for emphasis, we believe the major contributor to this inconsistency is our inability to get an exact duplication of each customer's solder reflow profiles. As such, the SSST results are not well suited for lot acceptance testing. However, SSST does provide a measure of differentiation between manufacturing batches. It will continue to play an important role in comparative evaluations of material and process changes. It will also continue to be used to evaluate failure rates reported by our customers whenever we can test comparable samples. These and future SSST applications may well hold the key to our efforts to eliminate power-on failures.

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