

Improved SMT Performance of Tantalum Conductive Polymer Capacitors with Very Low ESR

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Abstract

KEMET Electronics Corp has implemented several process and material improvements in order to improve the surface mount (SMT) performance of low ESR conductive polymer tantalum capacitors. This includes large case size (up to 7343-43) capacitors with ESR as low as 5 m Ω . Six Sigma methodologies (DMAIC: *define-measure-analyze-improve-control*) were used to structure the improvement process. This paper describes the project goals (define phase), new measurement techniques that had to be developed (measure phase), the conceptual model to explain SMT failures (analyze phase), process and material improvements (improve phase), and new control measures put in place (control phase).

Introduction

Capacitors serve numerous functions in the electronic devices on the market today. These functions include filtering, tuning, energy storage, voltage modulation, etc. In many of these applications the number of components required to meet the circuit design criteria is determined by the capacitance and ESR of the capacitor¹. In applications such as output filters on switch mode power supplies industry trends toward lower circuit voltages operated at higher frequencies and higher current demands are driving the demand for low ESR, high capacitance components.

Several other characteristics of the capacitor are important to the circuit designer. High surge currents are inherent in the applications which require low ESR capacitors. The use of an external resistance placed in series with the capacitor to reduce the surge current is not an option. The capacitor must have the ability to withstand high current surges without the benefit of resistance added elsewhere in the circuit.

Miniaturization of electronic devices, especially in the consumer electronics industry, continues unabated. Components with high volumetric efficiency are required to continue the trend toward smaller, more

highly functionalized lap tops, cell phones, and other portable communication devices.

Tantalum capacitors utilizing an intrinsically conductive polymer as the solid cathode electrolyte provide low ESR, high capacitance, volumetric efficiency, and excellent ability to withstand high surge currents. These capacitors provide the lowest cost solution to meet the design requirements for several applications.

Recent European legislation (RoHS- Restriction of Hazardous Substances) has fueled the push in the industry for Pb free components. Removing the lead from surface mount tantalum capacitors was not a problem (although many high reliability customers are very concerned about the potential for tin whiskers with 100% tin coated terminations). However, in order to be a Pb free capable device the component must be able to withstand the higher surface mount temperatures customers use to attach the components to boards using Pb free solders.

Strategies utilized to manufacture ultra low ESR tantalum capacitors have been described previously². In order to enhance the reliability of low ESR conductive polymer tantalum capacitors during a Pb free solder process, Kemet utilized a Six Sigma process improvement methodology. This paper describes how Kemet applied this methodology to improve the SMT performance of conductive polymer tantalum capacitors to meet the requirements of a Pb free board mount process.

Six Sigma Method

The six sigma process improvement process is generally broken down into five phases referred to by the acronym DMAIC: define, measure, analyze, improve, and control³. The goals of the project are specified in the design phase. In the measurement phase existing tools for measuring key metrics required to achieve the objectives specified in the define phase are analyzed to insure they are valid and reliable. The existing measurement tools are improved and new

tools developed as needed based on measurement system analysis. In the analyze phase experiments are run to identify ways to eliminate the gap between the current performance and the desired goal. Additional experiments are run to optimize the levels of the key factors impacting performance in the improve phase. Improvements to the process are institutionalized by incorporating them into operating procedures, raw material specifications, control charts, etc. in the control phase. Throughout the project statistical tools are used to analyze the data and determine if the differences in the data are real, or can be attributed to random variation.

Define Phase

The voice of the customer was critical to establishing the goal of the project. A Quality Function Deployment tool (QFD) was used to select the goal. A QFD provides a structure for ensuring that customer's needs and wants are heard, then directly translated into project goals. Based on the input from key customers and distributors the project team decided to focus on eliminating SMT shorts during a Pb free mounting process.

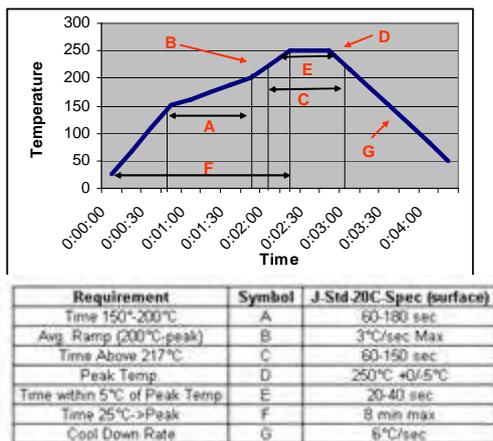


Figure 1. Pb free mounting profile specification.

Customers demand both low ESR and high reliability, so ESR performance could not be compromised. From the QFD, the goal of the project to eliminate SMT shorts from all of Kemet's conductive polymer products was identified. This includes Kemet's T530 multiple anode series with industry leading ESR levels below 5 mΩ, and T520 series of single anode capacitors with ESR levels as low as 7 milliohms. From the various phases of the QFD, the technical requirements, critical part and process characteristics, and process control methods were identified to meet the goal.

Measure Phase

Prior experience with conductive polymer had demonstrated the relationship between polymer

coverage and SMT performance. This relationship can easily be demonstrated by intentionally applying thin external conductive polymer coatings to capacitors and monitoring leakage performance before and after board mounting. Although polymer coverage was known to be a critical characteristic impacting SMT performance, no quantitative measure of polymer coverage was known. In-house experts were consulted to develop a tool to reliably measure polymer coverage. This tool was critical to the effort to improve polymer coverage and ultimately SMT performance. Once a tool for measuring polymer coverage was developed, measurement system analysis (MSA) was run to insure the new measurement system was adequate.

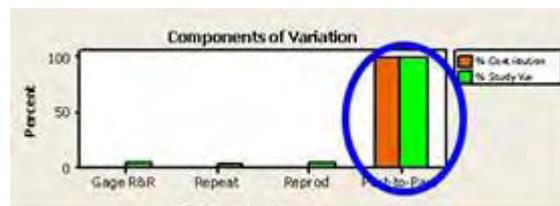


Figure 2. Gage R&R results for polymer coverage measurement system.

Due to the low ppm failure rate for SMT shorts, large sample sizes are required to measure SMT performance directly. Since the SMT test is a destructive test (once parts are mounted to a board they can not be removed from the board and sold to customers), a method for measuring differences in SMT failure rates without mounting was required. A non-destructive simulated SMT test was developed to allow the project team to evaluate potential process changes. The simulated SMT test is represented schematically in Figure 3.

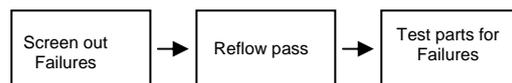


Figure 3. Schematic representation of simulated SMT test.

In order to accurately simulate board mounting the temperature profile of the reflow oven is modified during a simulated SMT test to compensate for the lack of a test board which acts as a heat sink during actual board mounting. A thermocouple was placed inside the molded case to measure the temperature of the capacitor within the case during the reflow pass. The reflow oven heaters were adjusted so the capacitor was exposed to the desired temperature profile.

In an effort to prioritize the improvement effort a failure site density map was constructed during the analyze phase of the project. The classical method of leakage failure site identification is to strip away the molded case and apply a negative bias to anodes in a dilute solution of copper sulfate. Leakage sites are

identified by looking for places where copper plates onto the anode. However, this method was found to be unreliable. A new procedure was developed to allow the location of failure sites to be identified. The application of a very high current for sufficient time causes the anode to discolor at the failure site as it heats up due to Joule heating. After stripping away the molded case the location of the failure site can be identified. A program was written to control the voltage applied to a failed part based on the leakage current. The program starts at 1 volt and slowly ramps to the voltage where the current exceeds 3 amps. It holds for 5 seconds then discharges. Once discharged, the epoxy case, lead frame, and external cathode layers are stripped away using acid solutions revealing the failure site.



Figure 4. Picture of Stripped Capacitor Revealing Failure Site at Top Edge of Anode

As will be discussed further in the section describing the analyze phase, the leakage site density map indicated the bulk of the failures were located on the edges of the anodes. To drive the effort to reduce the sensitivity of the edges of anodes to mechanical stress a method for measuring edge sensitivity was developed.

An apparatus was designed and fabricated to measure the force applied to the edge of an anode while measuring the leakage of the capacitor. Electrical contact to the edge of the anode is established through a pad mounted at a 45° angle to the edge of the anode as shown in Figure 5. A predetermined level of force is applied to the edge of the anode using a Chatillon force gage. Rated voltage is applied to the anode and the initial DC leakage is read and recorded. The applied voltage is removed from the anode and the contacting pad is rubbed across the edge of the anode. Rated voltage is again applied to the anode and the DC leakage is recorded. If the leakage is less than that defined as a short, the applied force is increased in predetermined increments. At each new force setting the leakage is read before and after the edge is rubbed with the contacting pad. The force required to cause the part to short is recorded and the data generally plotted on a probability plot.

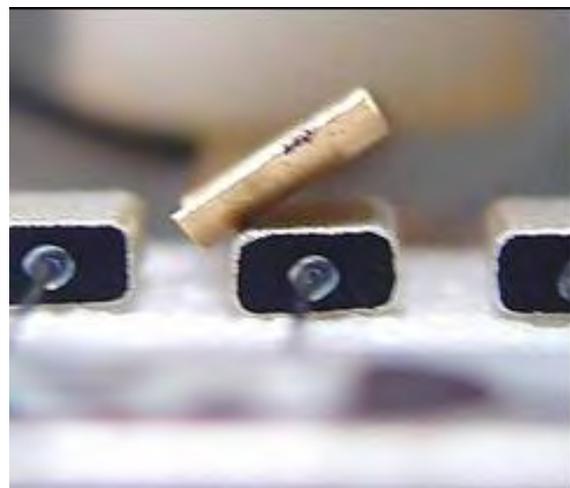
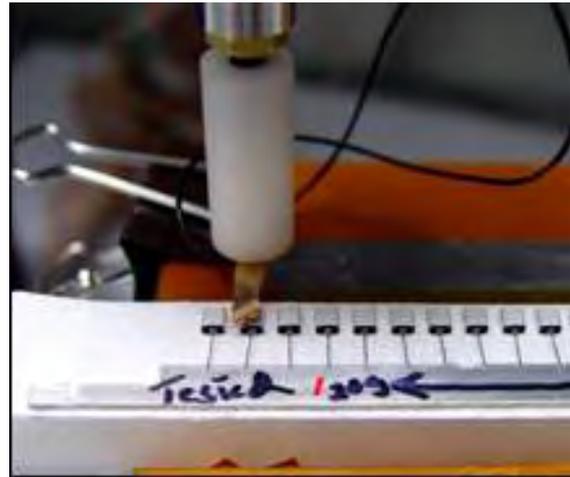


Figure 5. Prototype Edge Sensitivity Tester

A gage R&R study was conducted to determine if the test was reliable. This study indicated that 5.8% of the variability in test results was due to variation between successive tests by the same operator on parts pulled from the same group (repeatability). Variation due to differences between operators (reproducibility) accounted for 0.1% of the variability in the test results. The remaining variability was due to differences between the groups tested. This indicated the edge sensitivity tester could be used to drive efforts to reduce the susceptibility of parts to thermo-mechanical stress on the edges of the anode.

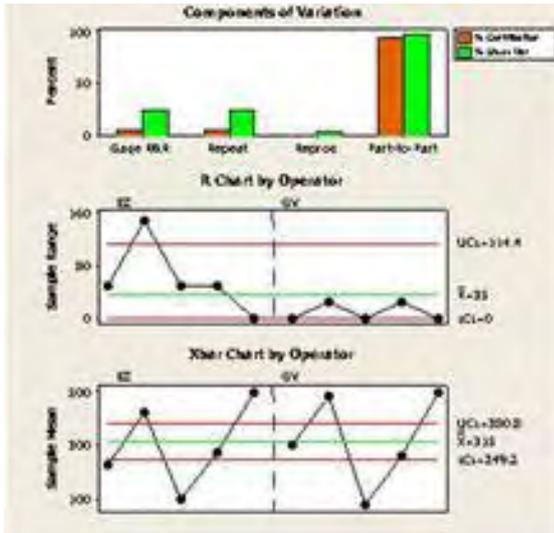


Figure 6. Results of gage R&R study on prototype edge sensitivity tester.

Analyze Phase

The goal of the analyze phase was to develop a conceptual model to describe the mechanism responsible for SMT shorts and highlight opportunities for improvement in the improve phase of the project. Thermo-mechanical stresses resulting from differences in coefficients of thermal expansion of the various materials used in the construction of a tantalum capacitor have long been postulated as the cause of leakage failures at SMT⁴. In order to demonstrate the role thermo-mechanical stress plays in SMT leakage failures, an experiment was run during the development of a new part type. This part type was a particularly challenging part type due to several factors including the voltage rating, ESR specification, CV, and geometric requirements. The SMT failure rate at this stage in the development process was still quite high (>1000 ppm). Leakage was measured on a batch of parts prior to encapsulation of the anode in a molded case. The batch was passed through a reflow oven and leakage was read again. Virtually no change in leakage occurred as a result of the reflow pass. The batch was then processed through the encapsulation and aging processes. The parts were screened to ensure any leakage failures incurred as a result of the encapsulation process were removed. Following the screening process the batch was sent back through a reflow oven. During the post reflow leakage screen several failures were detected.

CTE (ppm/°C)	Epoxy	Ta anode
Alpha 1	25	7
Alpha 2	75	7

Table 1. Typical coefficients of thermal expansion for a tantalum anode and mold epoxy used to encapsulate surface mount capacitors.

John Prymak hypothesized that the mismatch in coefficients of thermal expansion (CTE) between the epoxy molded case and the tantalum anode could result in thermo-mechanical stress on the anode during the cool down phase of SMT⁵. In order to confirm John's hypothesis a series of experiments were run during which leakage current and temperature were read as capacitors traveled through a reflow oven setup with a Pb free mounting profile. A thermocouple placed in a solder joint on a surface mount test board was connected to a data logger which recorded the temperature during the reflow pass. A very high temperature solder was used so that the solder would not reflow during the reflow pass. Half rated voltage was applied to singulated capacitors on a lead frame strip by attaching clips to the lead frame and running connecting wires to a power supply. The leakage current was recorded by measuring the voltage drop across a 1K Ω resistor in series with the strip and power supply as the strip of parts and surface mount test board were passed through the reflow oven simultaneously. A plot of leakage versus temperature for the majority of parts exhibits an exponential correlation as shown in Figure 7a. Figure 7b is a plot of a capacitor which failed during the test. Although very few capacitors failed during these tests, all failures which did occur, failed during the cool down phase of the reflow pass. These results confirm the hypothesis that CTE mismatches in the construction of a tantalum capacitor play in SMT leakage failures. The team concluded that a low CTE mold epoxy was needed to reduce these failures. During the improve phase the team worked closely with an epoxy supplier to develop a formulation suitable for this application.

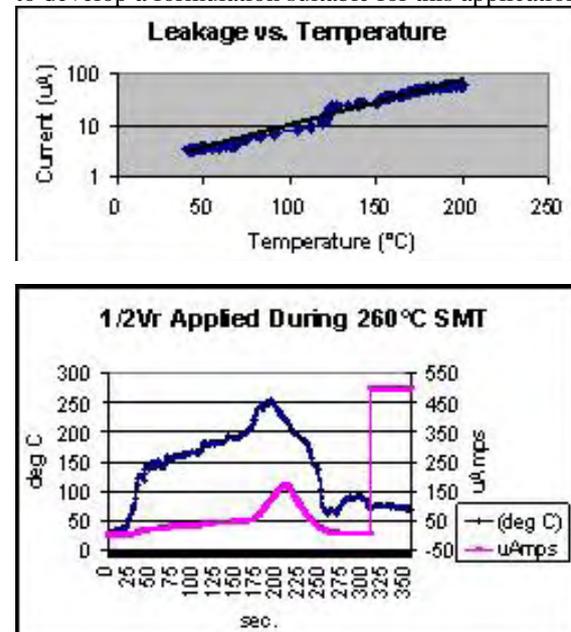


Figure 7. Plot of leakage versus temperature during heat up of a typical part showing exponential correlation (a) and leakage versus temperature of a part that failed during the cool down after reflow (b).

In order to gain an understanding of other factors that might contribute to SMT shorts, SMT failures generated during in-line testing are routinely submitted for failure analysis. One element of the failure analysis was to determine the location on the anode of the failure sites. As described in the measure phase a method was developed to allow the team to determine the location of failure sites on the anode. Information from the failure site analysis is stored in a database. In addition to documenting the location of the failure site the database contains information on part type, lot number, and critical process and material set information. Analysis of the data in the failure site database allowed the team to construct a failure site density map. The failure site density map indicated the majority of failures occurred on the edges and corners of the anode. This finding is consistent with the role that CTE mismatches play in SMT leakage failures, since the greatest stress during thermally induced expansion and contraction occurs on corners and edges. In addition to reducing the stress on the edges by reducing the mismatch in coefficients of thermal expansion of the anode and molded case, this analysis highlighted the need to reduce the sensitivity to stress on the edges through material and process improvements during the improve phase of the project.

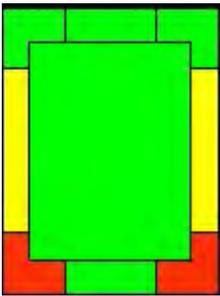


Figure 8. Example of a failure site density map for SMT shorts. Red indicates areas of high failure density on bottom corners; yellow moderate failure density on side edges; green low failure density.

An important characteristic of the intrinsically conductive polymer, which serves as the primary cathode material in ultra low ESR solid electrolytic capacitors, is the ability to transform to a less conductive state in the vicinity of a leakage site due to Joule heating. This characteristic of the intrinsically conductive polymer is responsible for the healing mechanism of these capacitors. The carbon and silver contained in the subsequent layers of a tantalum capacitor construction do not possess this property. If the carbon or silver come in contact with the dielectric the capacitor will be a short. A thin or porous primary cathode layer can allow carbon or silver to penetrate to the dielectric layer as these layers move due to expansion and contraction during the SMT process. In order to demonstrate that a thin conductive polymer layer can result in an increase in shorts at SMT the

standard process was modified to generate parts with reduced levels of external polymer buildup and processed through a simulated SMT process as described previously. The results from this experiment are plotted in Figure 9.

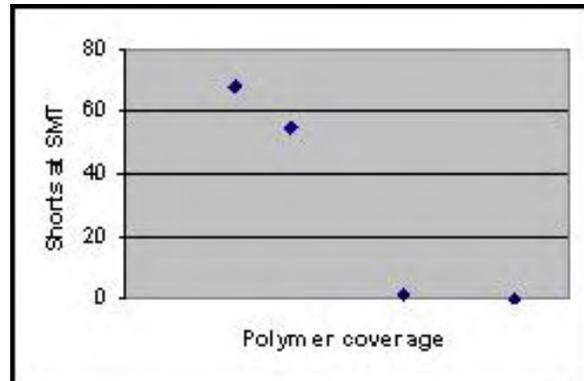


Figure 9. Plot of SMT shorts versus polymer buildup

In order to better understand the sources of variation in polymer coverage a components of variation (COV) study was conducted. The initial study determined the relative importance of variation:

- between anode lots
- within anode lots
- between formation lots
- between conductive polymer lots
- within conductive polymer lots.

Follow-up COV experiments further narrowed the source of variation in polymer coverage to specific steps in the manufacturing process. Comprehensive process maps of these steps were generated to assist in the identification of possible factors to be considered during the improve phase of the project.

Improve Phase

The analyze phase of the project pointed to several opportunities to improve the SMT performance of Kemet's low ESR conductive polymer products:

- Optimize the anode design to better withstand the thermo-mechanical stress of SMT
- Improve the polymer coverage
- Reduce variation in polymer coverage
- Develop materials and processes to reduce the susceptibility of the edge of the anode to thermo-mechanical stress
- Reduce thermo-mechanical stress on the anode by more closely matching the CTE of the tantalum anode and the molding epoxy used to encapsulate the anode
- Implement an in-line Pb free reflow profile to pre-stress capacitors

The analyze and measure phases of the project laid the foundation for improving polymer coverage in the improve phase. The process maps and QFD helped investigators select factors to be investigated further in

a series of designed experiments (DOE). The ability to quantify polymer coverage allowed the results of the DOE's to be analyzed objectively using a statistical analysis software program. As a result of these experiments several process modifications were identified which resulted in improved polymer coverage.

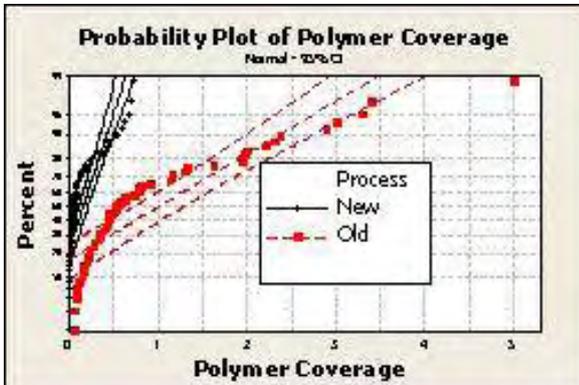


Figure 10. Probability plot of polymer coverage before and after improvements

In addition to identifying process factors to be considered in order to improve polymer coverage, the process maps developed during the analyze phase identified key raw material characteristics to be investigated. Although all of the materials were within the raw material specifications, a control chart of the variability of a critical raw material characteristic revealed the presence of non-random variation in incoming lots of material. The raw material supplier was contacted and information requested regarding the capability of their manufacturing process. These discussions led to a new, tighter raw material specification based on the capabilities of the supplier's manufacturing process. Other characteristics of the raw material specification were reviewed and tightened based on the supplier's process capability.

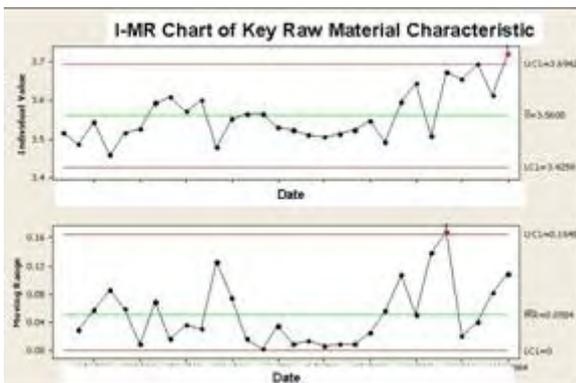


Figure 11. Control chart of critical raw material characteristic indicating the presence of non-random variation.

The team worked closely with raw material suppliers to develop new carbon and silver formulations to improve the edge sensitivity of conductive polymer capacitors

without degrading ESR performance. A series of DOE's were run to investigate resin chemistry, resin to conductive filler ratios, conductive filler particle size distributions, etc. As a result of these DOE's new carbon and silver formulations were developed with reduced edge sensitivity and lower ESR following Pb free mounting profiles. Hypothesis testing was employed to demonstrate the differences in performance between the old and new carbon and silver formulations were statistically significant.

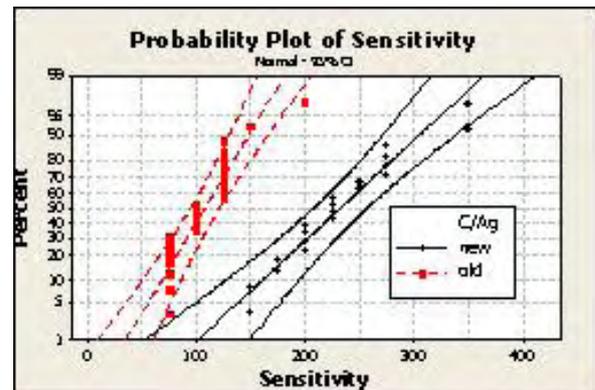


Figure 12. Edge sensitivity probability plot for improved carbon/silver formulation

The team also worked closely with the supplier of epoxy molding compound to develop a low CTE formulation suitable for this application. Although experiments in the analyze phase had indicated that mismatches in coefficients of thermal expansion between the various elements of the capacitor were responsible for SMT leakage failures, several other factors must be considered when reformulating the molding compound. These factors include glass transition temperature, moisture adsorption characteristics, shrinkage, shelf life, cost, printability, lead frame adhesion, and color to name a few. The results of designed experiments were statistically analyzed and process factors most critical to consistent high quality mold epoxy were identified. Control charts of critical characteristics were established and monitored to ensure consistent product was manufactured.

Solid electrolytic capacitors are typically subjected to an in-line reflow pass to pre-stress the anodes prior to the final customer packaging operations. In order to meet the new lead free requirements these in-line reflow profiles had to be modified to correspond to a lead free profile. Material and process improvements were required to minimize the ESR shift during the higher in-line reflow pass. As a result of the work of the Six Sigma SMT Improvement team and the ESR reduction team a 10 fold reduction in SMT shorts was achieved while continuing to drive ESR for single anode capacitors below 7 mΩ.

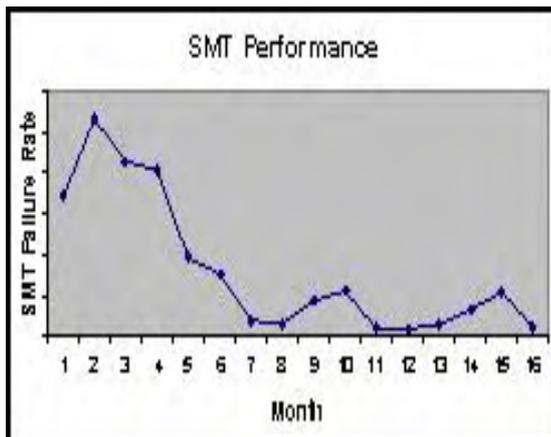


Figure 13. Improvement in SMT performance

Control Phase

The SMT Improvement Team continues to utilize Six Sigma tools to further reduce SMT shorts as part of Kemet's commitment to continuous quality improvement. However, it was vital that the improvements already realized were incorporated into operating procedures, raw material specifications, control charts, etc. Raw material specifications of all critical characteristics have been reviewed and the raw material specification modified based on the suppliers process capability. Process improvements have been incorporated in operating procedures and training programs. Internal reports have been written to document the work carried out by the team. These reports document both what has been learned and the limitations of what has been learned, to serve as the basis for further improvements. Control charts of critical process characteristics have been established, both internally and by raw material suppliers. In most cases these control charts track characteristics whose impact on SMT performance was not previously recognized or which could not previously be quantified.

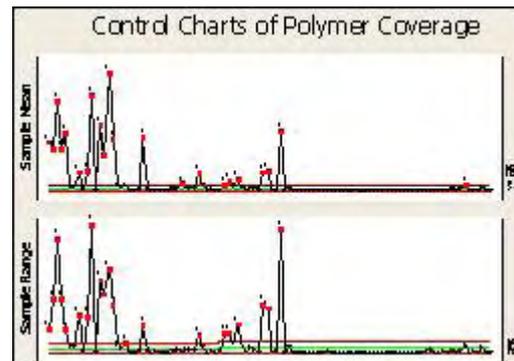


Figure 14. Control chart of polymer coverage.

Conclusions

KEMET Electronics Corp has utilized Six Sigma improvement methodologies to reduce SMT shorts by an order to magnitude. Only 2 or 3 tantalum capacitor manufacturers in the world have the technology required to produce capacitors with single digit ESR levels, leading edge cap and voltage ratings, and outstanding SMT performance. Through the use of Six Sigma methodologies Kemet intends to remain a technology leader in these areas.

References

1. E. K. Reed, J. C. Marshall, and John Prymak, "Lowest ESR Tantalum Chip Capacitor," Proceedings of the 18th Capacitor and Resistor Technology Symposium, p. 22 (1998)
2. R. Hahn and K. Pritchard, "Strategies for Manufacturing Ultra Low ESR Ta Capacitors," Proceedings of the 18th European Capacitor and Resistor Technology Symposium, p. 166 (2004)
3. T. Pyzdek, "Six Sigma Handbook" McGraw-Hill Company, 2003
4. D. M. Edson and J. B. Fortin, "Improving Thermal Shock Resistance of Surface Mount Tantalum Capacitors," Proceedings of the 14th Capacitor and Resistor Technology Symposium, p. 169 (1994)
5. J. Prymak, "Power-On Failures in Tantalum and Aluminum SMT Capacitors," Proceedings of the 22nd Capacitor and Resistor Technology Symposium, (2002)