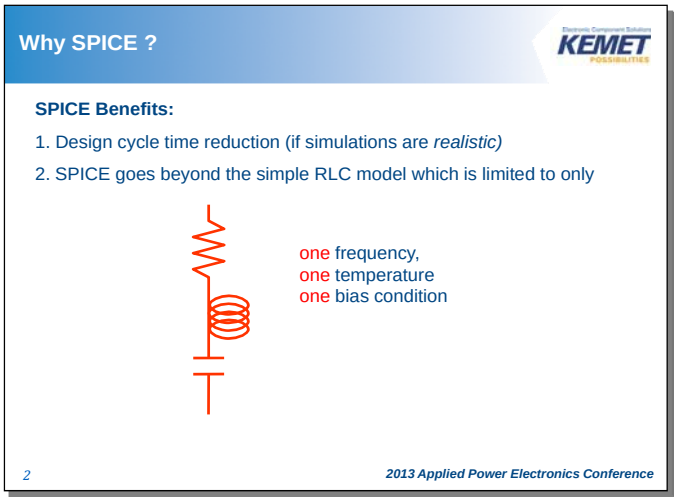
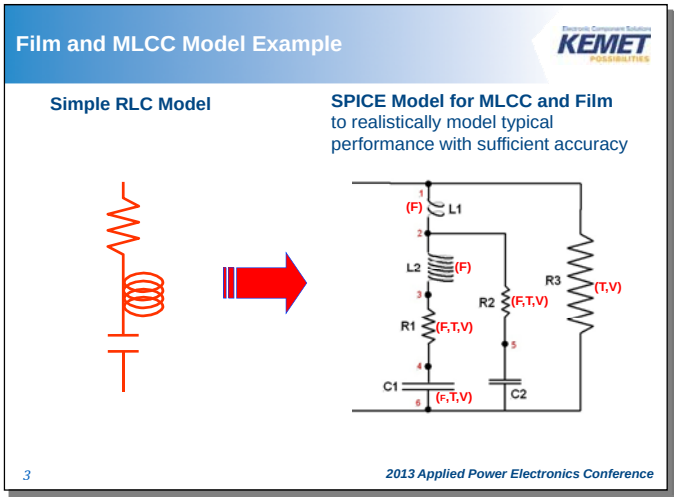
Almost all capacitor manufacturers are supplying models or software to show expected performance of their devices over frequency.



The advantage of Spice is reducing design time. Every capacitor has some parasitic resistance (ESR or Equivalent Series Resistance) and parasitic inductance (ESL or Equivalent Series Inductance). To model a capacitor with no ESR or ESL would create a response that no capacitor can achieve. Replacing the perfect, "ideal" capacitor with the simple RLC recognizes the parasitic elements of resistance and inductance, but this model is valid for one frequency, one temperature, and zero volts DC bias.



Here is an example of replacing the simple RLC with slightly more complex model for MLCC or Film SPICE calculations. Additional capacitive, resistive, and inductive elements are included.

The resistive, capacitive, and inductive elements may be factored by frequency (F), temperature (T), and DC bias (V) for ceramics (depending on dielectric).

Ceramic and film capacitors have minor frequency impacts on capacitance, with slightly increased effects on X5R, X6S, X7R, X8L, and higher K dielectrics (Z5U and Y5V).

For C0G type ceramics, the capacitance is not factored by bias, and minimally factored by temperature. The X5R and X7R dielectrics can lose 15% of nominal capacitance over temperature while the higher K (Z5U and Y5V) can lose nearly 60% of the nominal capacitance – all with no bias.

For DC bias, the C0G and most film have almost no impact, while for the higher K dielectric ceramics (X5R, X6S, X7R, X8L, Y5V, Z5U, etc.) the impacts can be substantial on capacitance(reductions of 80 to 95 percent from nominal values).

This model creates the first series resonance (or self-resonance, SRF) based on C1, R1, and L2. With R3 and C2 in parallel with C1-R1-L2 creates the first parallel resonance, and L1 in series with R2-C2 creates the second series resonance.

ESR as factored by Frequency

$$ESR_{fx} = ESR_{SRF} \times \left[1 + 10^{\left\{ Log_{10}\left(\frac{fx}{SRF}\right) - R_{Off} \right\}} \right]$$

SRF	-	self-resonant frequency
fx	-	test frequency
R_{Off}	-	Width factor typically 1.0 to 1.9

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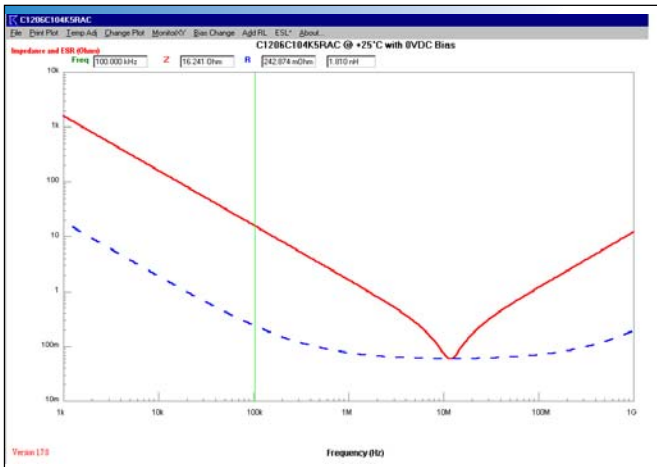
Here is the method by which the ESR is frequency modulated in our software. As the width factor (R_{Off}) increases, the flatness of the ESR response increases, and it becomes less flat or sharper as this factor decreases.



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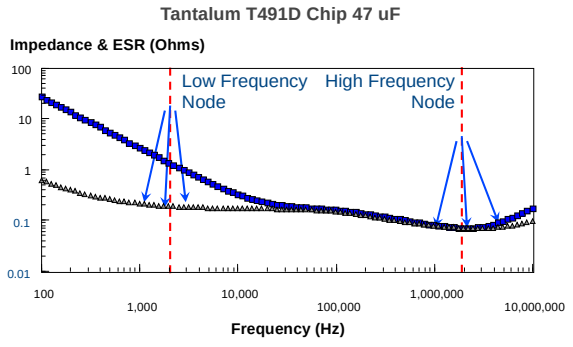
Here is a typical impedance and ESR versus frequency plot. For ceramic and film models there are twelve key seed values for each part type required to facilitate this response. The key values are manipulated to allow the calculated response to lie on top of the measured response. There are over 9,000 part types in KEMET Spice.

Electrolytic Frequency Scan



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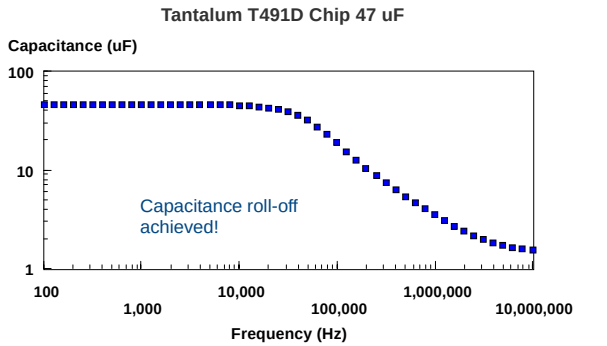
The ESR response of the electrolytic capacitors appears to have two nodes where the ESR reaches minimum values. One of the nodes appears in the lower frequency range and the other in the higher frequency range. There may be an additional step down from the low frequency node to the high frequency node.

Capacitance roll-off



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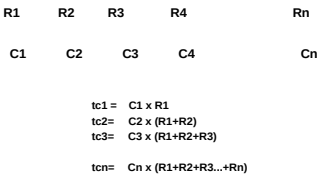
The measured capacitance of the electrolytics (and EDLC) appears to decay with increasing frequency. This decay or roll-off is very dependent on the capacitance value and the resistivity of the cathode materials.

Capacitance changes dramatically with frequency – the RC-Ladder



tc1 = C1 x R1
tc2= C2 x (R1+R2)
tc3= C3 x (R1+R2+R3)

tcn= Cn x (R1+R2+R3...+Rn)

- Device acts as RC-Ladder network.
- Capacitance decays as frequency increases.
- Calculating ESL based on capacitance and self-resonance frequency could lead to gross errors.

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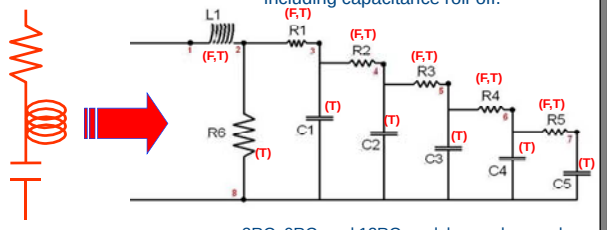
The RC-Ladder describes the roll-off effect, as the time constants for the deeper capacitive elements (Cn on the right) are much larger than of the shallow elements (C1 and C2 on the left). As frequency increases, these long time constants effectively eliminate the deepest elements, then progresses to the outside, losing capacitance with increasing frequency.

Aluminum and Tantalum (and EDLC) Model

Simple RLC Model

5RC-SPICE Model for electrolytic with 5 RC ladder elements to realistically model typical performance with sufficient accuracy, including capacitance roll-off.



3RC, 9RC, and 12RC models are also used

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Here is an example of replacing the simple 5RC circuit with aluminum or tantalum model display. The resistive and inductive elements may be factored by temperature and frequency, while the capacitive elements are factored only by temperature.

The RC-Ladder creates a capacitance roll-off versus frequency. There are also circuits of 3, 9, and 12 RC-Ladder element pairs. The lossier the capacitor, the deeper the chains of capacitor elements, and the higher the number of RC ladder element pairs.

Large tantalum, and aluminum polymer capacitors with very low ESR's may have only 3-RC ladder element pairs, while very lossy tantalum MnO_2 or EDLC capacitors will have 12 RC-element pairs. Some EDLC capacitors require up to 17 RC element pairs to effectively reproduce the capacitance roll-off effects.

The RC-Ladder also has an impact on the calculated ESR.

Frequency Adjustment for Esr

Low Frequency Node (Log10(f)) Flo

High Frequency Node (Log10(f)) Fhi

$$ESR_{fx} = ESR \times \left[1 + 10^{(Flo - Log(fx))} + 10^{(Log(fx) - Fhi)}\right]$$

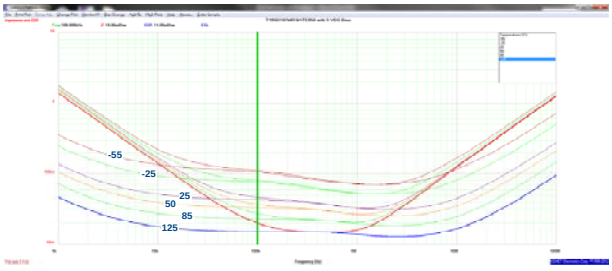
Flo and Fhi carried as seed values for each part number.

The frequency responses of ESR for the tantalum capacitors is based on the RC-Ladder model and in the values of resistance, inductance (based on case), and the two frequency nodes, creating seed values for each capacitor part number.

Here is how we manipulate the ESR for those two nodes in the frequency response. As we manipulate the lower seed value (Flo), the ESR back at 120 Hz is monitored to give us a realistic DF at 120 Hz. We manipulate the seed value for the upper node to give us a response close to the 10 MHz ESR measured. The base ESR is selected to define the minimum ESR and the ESR at 100 kHz.

Impedance, ESR Example: Tantalum

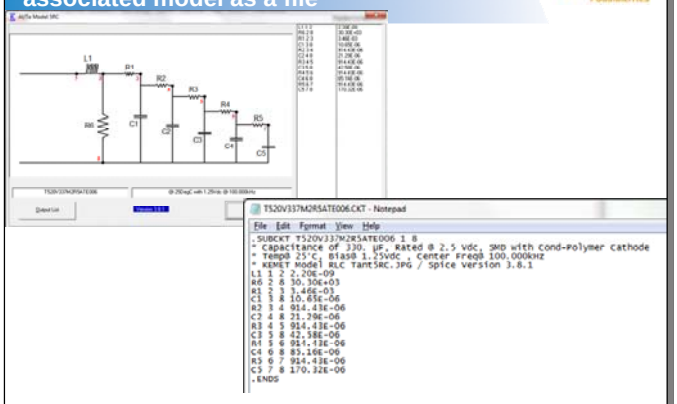
Typical T495 Impedance & ESR Frequency Response
@Bias 5Vdc, Temps of -55, -25, 25, 50, 85, 125 °C: T495D107M010ATE050



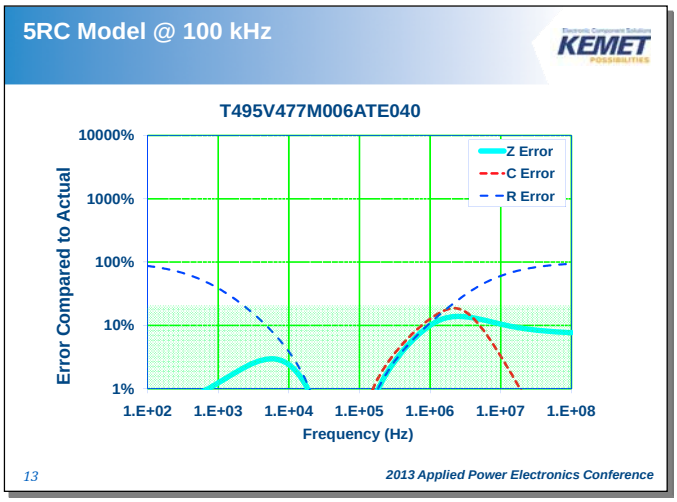
Ambient temperature, frequency, voltage can affect actual impedance and ESR depending on technology and dielectric

This is the impedance and ESR plot of a tantalum at -55°C, -25°C, 25°C, 50°C, 85°C, and 125°C temperatures, with 5Vdc rated voltage applied. The cursor is at 100 kHz and the readouts above the graph show the frequency, impedance, ESR, and ESL at 100 kHz for the selected plot (the 125°C plot).

Each part type can generate its associated model as a file



Here is the model and default ASCII file output for a tantalum-polymer device to show that the complexity of the model is dependent on the part type. There are 12 elements in this model while there were only 7 elements for the previous MLCC capacitor. The created ASCII files also define the temperature, bias, and frequency where these element values are captured. Because the model incorporates the RC-Ladder, variation of capacitance above and below the listed frequency will be factored by changing frequency, but the ESRs will not.

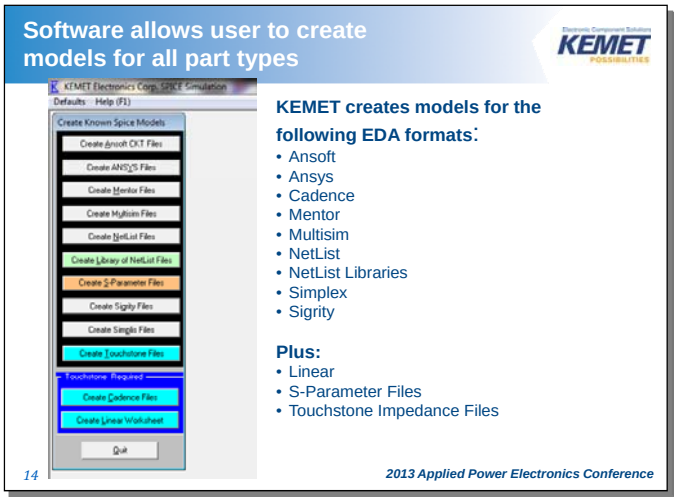


Here is the 5RC model where we calculated a frequency response based on the set model created at 100 kHz versus the actual response for varying frequencies

In the lower frequency range (100 kHz down to 100 Hz), the maximum Impedance error is only 3%. In the upper frequency range (from 100 kHz up to 100 MHz), the maximum error is less than 13%.

The Capacitance error in the lower frequency range is less than 1%. In the upper frequency range the maximum error remains below 20%, with half of that rage being less than 2%.

The ESR is acceptable (less than 20%) from 2 kHz through 2 MHz, but gets excessive (>20% error) outside that range. Without some adjustment for ESR, the only ESR change occurs as the capacitance decays.

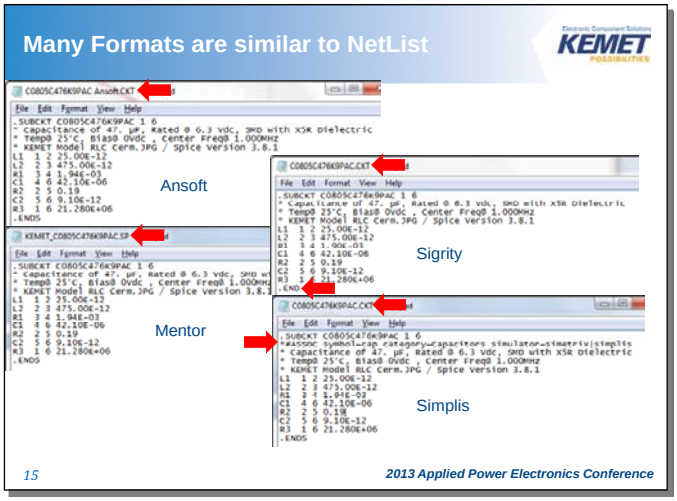


The KMET Spice software allows the user to generate any of the listed EDA model type for all or a limited number of part types. Specific EDA tolls include:

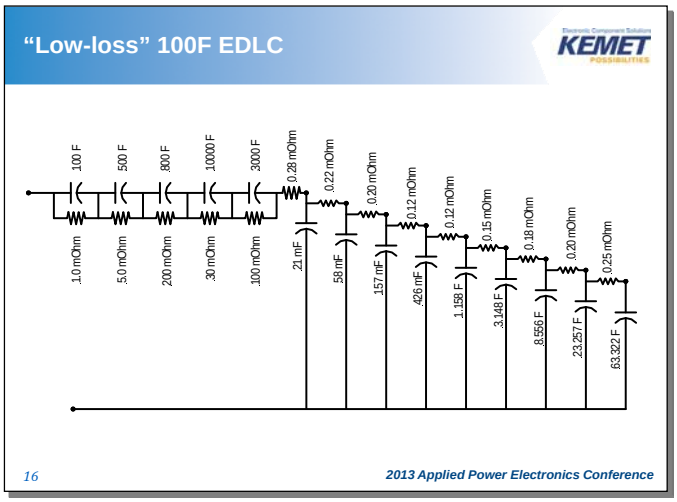
- Ansoft
- Ansys
- Cadence
- Mentor
- Multisim
- NetList
- NetList Libraries
- Simplex
- Sigrity

Plus:

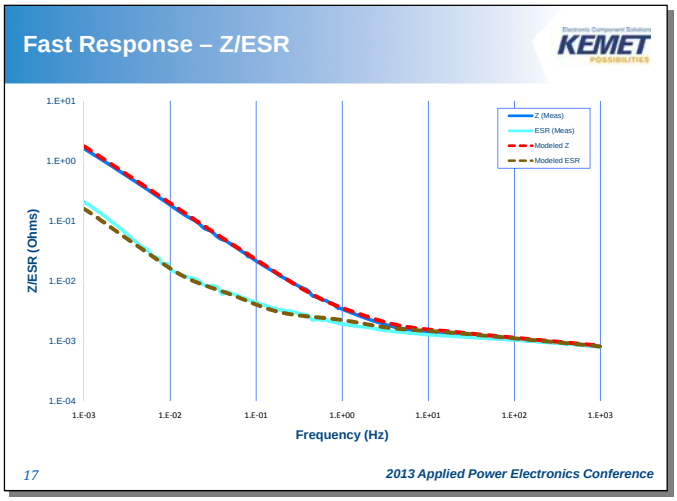
- Linear
- S-Parameter
- Touchstone Impedance



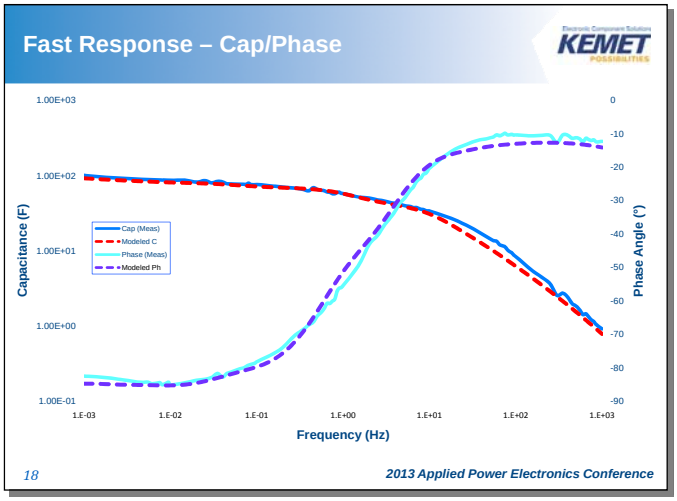
Similar to the NetList format are the Ansoft, Mentor, Sigrity, and Simplis models. The Ansoft, Sigrity, and Simplis are ".CKT" file types while the Mentor is a ".SP" file type. The Mentor requires the file name be prefixed by the component manufacturer, and the second line, or first comment line in the Simplis file defines the part as a capacitor, and polar if necessary. All the element values are the same.



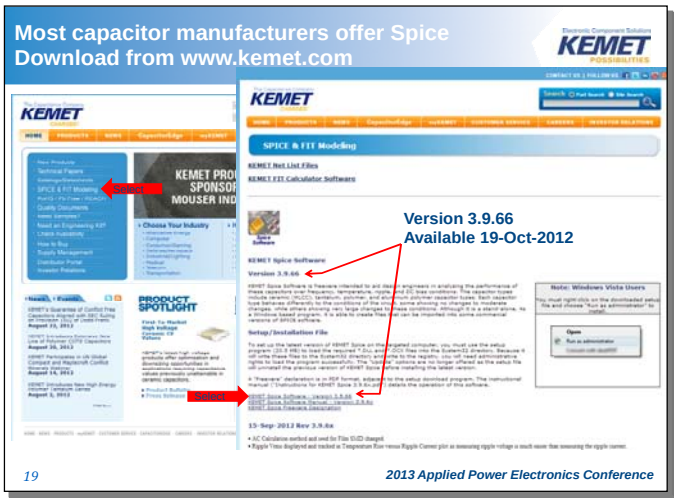
We have not added the EDLC to the software at this time, but we have completed preliminary work using MathCAD software. For this 100-Farad electrochemical double-layer capacitor, we not only created the 9RC ladder element, but also added a five pair RC network. The 5RC parallel network allows a frequency dependent ESR without any additional manipulation.



These are the measured and calculated responses of impedance and Esr for the EDLC. The correlation is excellent.



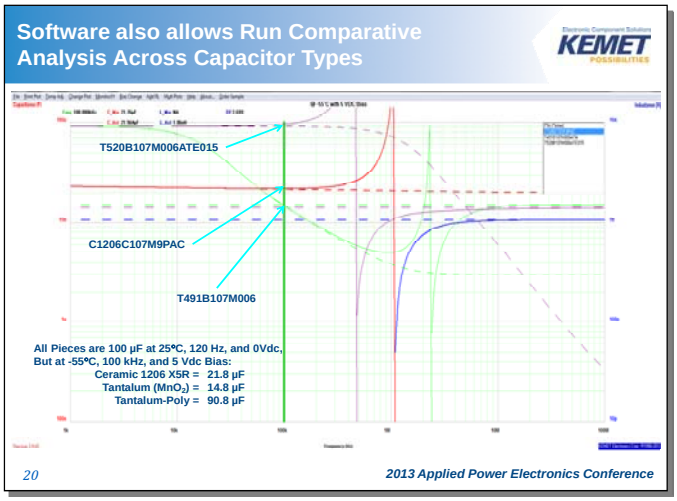
This plot shows the measured and calculated model response of capacitance and phase for the ECLC. Again, the correlation is excellent.



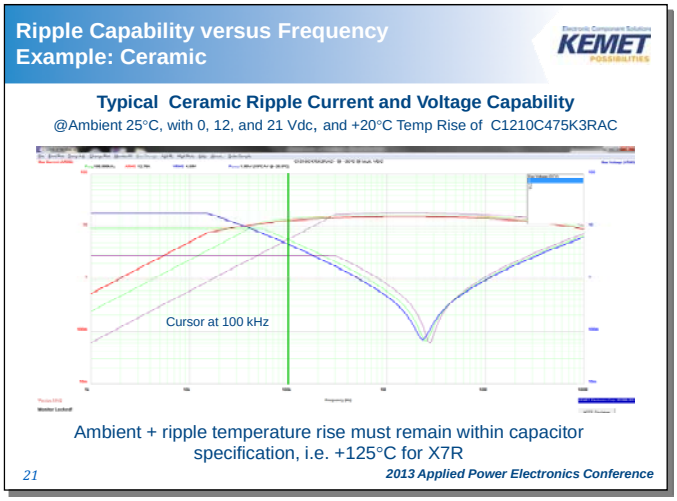
To download software, first go to www.kemet.com. Using main category of "SPICE & FIT Modeling" selection, "KEMET Software" page shows latest offering.

15-Sep-2012 Rev 3.9.6x (date of last major revision)

- Calculation method and seed for Film SMD changed. Ripple Vrms displayed and tracked in Temperature Rise versus Ripple Current plot.
- Ripple Vrms displayed and tracked in Temperature Rise versus Combined Multiple Ripple Current plots.
- ESR and Flo seed values adjusted in T491 & T494 to reflect last year's collected data for DF and ESR from production data.
- Corrected ESR seed values missing for T520A 47, 68, and 100 µF pieces.
- Expanded offerings, added T513, T540, T541, and T543.



In this plot of capacitance and inductance (ESL) versus frequency, we have a ceramic chip (C1206C107M9PAC) and a standard commercial tantalum with MnO_2, and a tantalum polymer. They are all of 100 uF at 120 Hz, and 25°C, with 0Vcd bias, but comparing these pieces at -55°C with 5Vdc bias at 100 kHz reveals that they can be very different. The commercial tantalum at -55°C has a substantial drop in capacitance such that it now measures only 14.8 µF, the ceramic is affected by temperature and voltage such that its capacitance now measures only 21.8 µF, and the tantalum polymer best retains its capacitance at 90.8 µF.



This is the plot of Irms and Vrms values versus frequency. Every capacitor has a specified power dissipation limit depending on case size and ESR. Power ($I^2 \times ESR$) causes internal heating and thus a rise in core and case temperature.

Note that ripple capability that achieves a +20°C temperature rise is not the limitation of the part, but rather an industry standard used for catalog entries.

Most ceramic and tantalum devices can run reliably with a 50°C temperature rise.

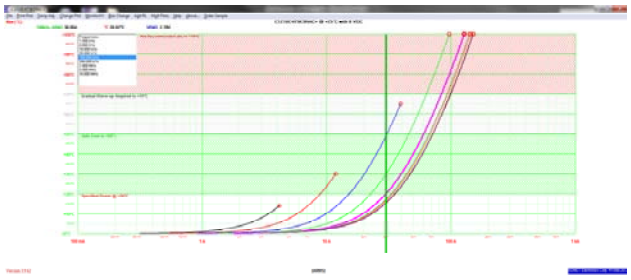
This becomes a limiting factor, as larger temperature rises will create large thermal gradients in capacitor structure.

Film capacitors have allowable rises (hot spot temperature) that vary with ambient.

Allowable temperature rise magnitude is suppressed as ambient temperature approaches maximum temperature.

Multiple Frequency Ripple Capability Example: Ceramic

Ceramic Temperature Rise at Multiple Freq. Capability
@Ambient 25°C, with 0 Vdc, and Temp Rise of C1210C475K3RAC



Ambient + ripple temperature rise must remain within capacitor specification, i.e. +125°C for X7R

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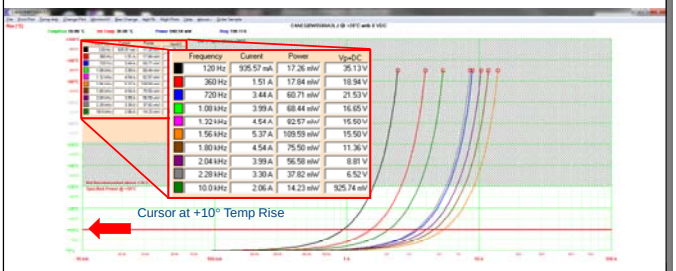
The calculation method for this plot of temperature rise versus applied ripple current is calculated differently from the previous plot. In this plot, incremental temperature rises are set, and the ESR at that elevated temperature is used to calculate the power. In the previous plot, the ESR at the ambient temperature is used, ignoring any ESR change created by the new internal temperature.

Temperature rise and Irms for up to 10 discrete frequency levels are available. Compared to the previous slide, this plot will result in higher current capability for devices, with negative TCRs throughout temperature rise. It will also result in lower current capability for devices showing any positive TCR in delta temperature range.

Temperature Rise @ Specific Frequencies and Currents, Example: Power Film

Typical Polypropylene Box Film
@Ambient 20°C, 10°C Temp Rise of C4AEGBW5500A3LJ



Ambient + ripple temperature rise must remain within capacitor specification, i.e. ambient 20°C + 10°C hotspot delta = 30°C internal

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The combined effects of several specific frequencies with associated ripple currents can be monitored with user selected temperature rise other than the default +20°C.

Example: DC-Link C4AE box series 50uF / 450Vdc with 10 ripple current frequencies allowing +10°C hot spot temperature. The maximum temperature rise would be 30°C as shown by the un-shaded bottom portion of the plot.

Thank You!