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How many capacitors can be balanced on the head of a pin? *Recent progress by the ceramic capacitor industry in downsizing now makes this more than a philosophic question. A more important question - the precision placement and soldering which is necessary to capitalize on component size reductions - is the subject of this month's Tech Topics. The author, Jim Bergenthal, is a KEMET Product Manager specializing in surface mount products.*

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Challenges in the Continuing Miniaturization of Surface Mount Resistors and Capacitors

by Jim Bergenthal

Introduction

Surface mount technology faces challenges from high lead count, fine pitch, integrated circuits, which use smaller and smaller passive parts in higher density assemblies. Some products would not survive without the benefits of high density and small size: disc drives, flash memory cards, lap top and palm top computers, video cameras, cellular radios, and various personal audio products. To meet these needs, many manufacturers offer resistors and capacitors in 1608 (0603) and 1005 (0402) chip sizes. Some manufacturers are even offering a 0502(0201) size, though there is little talk of using this size in any volume.

To successfully design and produce smaller sizes, the circuit designer, process engineer, part manufacturer, equipment manufacturer, and circuit board manufacturer must understand the critical factors determining success or failure. This article summarizes the tolerance stack-up conditions critical to success, and describes the factors leading to "tombstoning," the primary problem with mounting these chips. Finally, possible alternatives to the current soldering technology are discussed.

Present Status

Early analyses of resistor and ceramic capacitor use predicted a quick move to smaller and smaller chip sizes. The transition from 3216(1206) to 2012(0805) was expected to be an interim step to 1608 (0603), which in turn would progress rapidly to 1005 (0402) sizes.

The migration to smaller sizes has progressed more slowly than once predicted, primarily because the transition has proved costly and difficult. Some circuit assemblers have reached high volume production using 0603 chips; few have had similar success with the 0402 size. As with the early stages of surface mount technology, however, the trials of implementation have created a good understanding of the fundamentals necessary for success.

Surface mount technology (SMT) was developed as a tool for automated manufacturing. Its goal is for the p arts to end up on the circuit pads with a good solder fillet. Initially, SMT made repair much more complex, but as circuit assemblers learned more about process capabilities, repair technology began to develop. With experience it was found that some portion of the p arts' terminations could be off the pad and still yield good solder fillets and low PPM rates.

The introduction of 0603 and 0402 chip sizes has renewed the emphasis on the original goal and reopened the difficulties of repair. Experience has shown that the penalty for failing to mount these chips precisely on the circuit pads is a high rate of "tombstoning" and missed solder fillets. Repairing this size chip is a very difficult, if not impossible, proposition.

The Fundamentals: Tolerance Stack-up Conditions

Part Dimensional Tolerances

Part tolerances are a major factor in circuit pad design and surface-mount package design (tape and reel or bulk cassette). As chip dimensions shrink, tolerances have been reduced. Chip sizes 0805 and larger have a tolerance of ± 0.2 mm; smaller sizes must meet a tolerance of ± 0.1 mm. Furthermore, these tolerances will probably need further reduction (a target of ± 0.05 mm or less) to effectively apply chips of these sizes. This will place additional demands on part dimensional controls and termination developments.

Circuit Pad Design and Tolerances

To ensure that all parts are on the pad and have good solder fillets after the total process, all tolerance stack-ups must be considered in circuit pad design. The circuit pad must be large enough to ensure that terminations are placed on the pad all the time, yet must not be so large that solder adhesion forces contribute to tombstoning.

Circuit pad dimensions are determined by adding the circuit pad location tolerance to the placement machine tolerances. This figure is then multiplied by 2 and added to the maximum part dimensions. When this technique has led to large circuit pads (for 0805 sizes and above), some manufacturers have used smaller pads and allowed some terminations to be off the pads. Since this is not an option in small chips, all of these tolerances must be considered in pad design.

Artwork traces must enter the circuit pad at 180° only. Angled traces tend to contribute to rotational forces during solder melting, and possibly cause the chips to rotate off the pad.

Circuit Board and Pad Location Tolerances

To accurately place a chip, a placement machine must locate the circuit pad and place the chip directly on it. Placement equipment in use with 0805 sizes and above typically locate the chip by referring to a mechanically located zero point. The tooling pins on placement machines are inserted in tooling holes drilled in the circuit board. Common tolerances for the location of tooling holes relative to the circuit pad artwork are ± 0.2mm. The tolerances for pipette repeatability and reproducibility add another ± 0.05mm. To successfully place a smaller part, these tolerances must be all but eliminated.

Circuit board artwork tolerances can be reduced to less than ± 0.025mm through the use of fiducial marks on the board. Placement machines use video cameras to locate the 0,0 reference point at this fiducial. For smaller parts, a fiducial in multiple zones might be required. Some circuit assemblers have attempted to place 0603 chips without the use of fiducials by tightening the circuit board tooling hole tolerances. These have met with limited success.

Placement machine repeatability must be further reduced to less than 0.025mm. Some new placement machines anchor the table, tape, and reel transport rack to assist them in approaching these tolerances.

Packaging Tolerances

The mobility of small chips in the tape and reel cavity is a significant issue for placement equipment. Pick-up errors for 0603 and 0402 chips have been reported as high as 1000 PPM.

The movement of the chip in the cavity cannot be improved by a higher quality effort; it is related to the tolerance stack-ups between the minimum size chip and the maximum size tape cavity. The mini-

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mum size chip is the nominal dimension minus 0.1 mm; the *minimum* cavity must allow placement of the maximum size chip with a clearance of at least 0.05 mm. Taking all tolerances into account, the minimum size chip can move up to 0.35 mm in a maximum size cavity. For small chips, this is a significant figure.

To improve this, manufacturers are working to reduce chip tolerances. In addition, some of the newer placement machines have features that assist in reducing pick errors, such as video cameras to identify the center of the part in the tape cavity.

At this time, bulk cassette feeders appear preferable to tape and reel packaging for small parts. When the linear feeder is adjusted and secured, the pick-up error rate is lower than that of the tape and reel. However, linear feeders have a propensity to jam. To minimize this, manufacturers must improve the tolerances of the parts, and linear feeder technology must be improved. Another concern, which has not yet been extensively investigated, is potential damage to the parts from linear feeders.

Placement Machine Tolerance: Additional Concerns

When comparing placement machine efficiencies, it is important to remember that placement accuracy is critical.

Repeatable accuracy is critical to placing high-volume small parts. Fine-pitch placement machines placing integrated circuits operate at a much slower speed. To place 0603 and 0402 chips, high-speed "chip-shooters" will probably have to be run more slowly than advertised.

Some new placement machines look at the part when it is on the pipette, and adjust the placement location based on the center of the part. Some concern exists that low-mass parts will move on the pipette during high speeds, resulting in offset placement errors.

During pick-up, the location of the part in the tape cavity can also be influenced by the location of the tape and reel cassette in the transport system. Some placement machines are p lacing fiducials on the tape cassette; a video camera then looks for the fiducial and adjusts the pick-up point accordingly.

Tombstone Mechanics

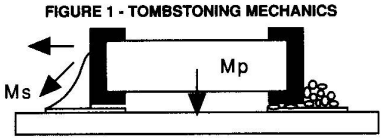
The biggest problem with small chips is that, because of their light weight, they tend to "tombstone" during the soldering process. (Table 1 contains a size and weight chart.) A chip "tombstones" when, secured by solder at only one end, it rises from its flat position on the pad to stand upright, resembling a tombstone.

Table 1 - PASSIVE PART DIMENSIONS (mm) & WEIGHTS (mg)

Resistors	Length	Width	Thickness	Weight
3216 (1206)	3.20	1.60	0.60	9.64
2012 (0805)	2.00	1.25	0.60	4.92
1608 (0603)	1.60	0.80	0.50	2.16
1005 (0402)	1.00	0.50	0.35	0.70
Capacitors	**Length**	**Width**	**Thickness**	**Weight**
3216 (1206)	3.20	1.60	0.90	12.00
2012 (0805)	2.00	1.25	0.90	6.50
1608 (0603)	1.60	0.80	0.80	3.50
1005 (0402)	1.00	0.50	0.50	1.40

Tombstoning occurs when the solder on one circuit pad transitions to the liquid state before the other, resulting in a moment about the solder joint. The counteracting moment is a function of the part's weight, and is located at the center of the part. (The equations for this process are shown in Figure 1.) Table 2 details the value of these moments for different chip sizes, and contains the Tombstone Ratio calculation, which measures the likelihood of a chip to tombstone given unequal soldering conditions. The greater the ratio, the more likely tombstoning will occur.

FIGURE 1 - TOMBSTONING MECHANICS



$Ms = Fo (\cos\varnothing)\ t$
$Mp = g\ (L/2)$

Table 2 - TOMBSTONE MOMENTS & RATIOS

Resistors	Solder Adhesion Fo (gf)	Moments Fo*cos45*t (*10-3)	Moment p g*1/2(*10-3)	Tombstone Ratio (Ms/Mp)
3216 (1206)	0.08	3.39	1.54	2.2
2012 (0805)	0.0625	2.65	0.46	5.4
1608 (0603)	0.04	1.41	0.17	8.2
1005 (0402)	0.025	0.62	0.04	17.7
Capacitors	**Solder Adhesion Fo (gf)**	**Moments Fo*cos45*t (*10-3)**	**Moment p g*1/2(*10-3)**	**Tombstone Ratio (Ms/Mp)**
3216 (1206)	0.08	5.09	1.92	2.7
2012 (0805)	0.0625	3.96	0.65	6.1
1608 (0603)	0.04	2.26	0.28	8.1
1005 (0402)	0.025	0.88	0.07	12.6

Several factors determine the propensity of a chip to tombstone. The amount of solder, for example, must be almost equal on both pads. If it is not, the moment forces will be unequal.

Process control variables for solder printing include:

- solder paste metal particulate shape and size
- solder stencil side wall shape
- solder stencil blinding
- location of the solder stencils relative to the circuit pad
- oxidation of solder paste metal powders.

The soldering process is also critical to minimizing tombstoning. The solder on both circuit pads must transition to the liquid state simultaneously. The type of solder process used greatly affects this. Processes under investigation include convection reflow and hot gas reflow, which have better uniform temperature distributions. Vapor phase reflow is also being investigated and is considered by some a leading candidate, particularly if some of the lower reflow temperature solders become viable.

The soldering profile is another key variable. Most success has been found with profiles that have very gradual preheat ramps. The objective has been to add preheat until all parts of the board are just below the liquidus point of the solder (+175°C). The final temperature rise then drives the peak temperature to a uniform low point above the liquidus point (+200°C). However, in this profile the circuit board remains above its glass transition temperature for a relatively long time, which creates some concern. A slow cooling ramp is needed to minimize stress build-up in the circuit assembly.

Future Developments

Surface-mount technology is constantly progressing. The challenges that once seemed insurmountable suddenly appear trivial, and new concerns arise to take their p lace. In the area of small chip placement, recently announced advances in glue placement accuracy and dot size control suggest that gluing chips to the board might be practical. Could a process such as solder paste rescreen/glue dot dispense/part placement work? If the glue were cured in the early stages of the reflow profile, holding the chip in place, and then solder were reflowed, would tombstoning be minimized?

The use of miniature resistors and ceramic capacitor chips is in its infancy. As the industry becomes more aware of the refinements needed to every element of these products, the technology will mature to accommodate the ever-greater precision required for small parts. The emerging question appears to be ***What is the smallest size practical?***

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