

Unlike electrolytic capacitors, where dielectric thicknesses can be set almost at will, the thinness of the dielectric layer of multilayer ceramic capacitors (MLCs) has historically been determined by manufacturing capability. As manufacturing capabilities improve, thinner dielectrics become available and voltage stresses under use conditions increase.

While these voltage stresses remain very small compared to those of electrolytic capacitors, they are sufficient to induce substantial secondary effects in the characteristics of the ferroelectric polycrystalline dielectrics of MLCs.

Some of the electrical peculiarities of MLCs with thin dielectric layers are discussed in this edition of Tech Topics.

Dr. John Piper
Vice President – Technology

Some Electrical Characteristics of Thin Dielectric (Low Voltage) MLCs

The capacitance equation is well known:

$$\text{Capacitance}(C) = \frac{kA}{t}$$

where **k** is the dielectric constant
A is the electrode area
t is the dielectric thickness

To achieve economies in size and cost, the thickness of the dielectric layer in electrolytic capacitors has, since their inception, been carefully tailored to be the minimum necessary to meet the manufacturer's expectations for voltage stress capability in life tests, voltage surges, etc. The strict dependence of dielectric thickness to maximum applied anodizing voltage makes easy the manufacture of electrolytic capacitors with any chosen dielectric thickness within a broad process range.

The voltage stress on the dielectric layer of a typical multilayer ceramic capacitor at its rated voltage is about one percent of the stress at rated voltage on the dielectric of a solid tantalum or aluminum capacitor. Additionally, ceramic capacitors are usually used at a small fraction of their rated voltage. So, as shown by the equation, reductions in dielectric thickness offer a major opportunity to increase nameplate capacitance per unit of volume or cost.

However, unlike the dielectrics of tantalum and aluminum capacitors, most MLC dielectrics are polycrystalline and ferroelectric so their electrical properties exhibit a strong dependence on applied voltage stress and temperature.

The individual ceramic layers of a MLC are made by forming a slurry of ceramic particles into the layer which is then sintered to make the dielectric. So, whereas, the anodized dielectric of a solid tantalum capacitor is a thin, conformal, amorphous film, the MLC dielectric is a relatively thick, highly structured, sintered layer of crystalline grains. The opportunity for mechanical imperfections, existence of grain boundaries, and property variations grain-to-grain all result in an inhomogeneous dielectric layer where the inhomogeneities cause localized electric fields much larger than the simple ratio of applied voltage to the overall dielectric thickness. It is usually these localized areas of high electric field, which cause voltage breakdown-type failures, e.g. life test, and voltage surge failures.

So, one set of considerations is the ability of the MLC manufacturer to make thin dielectric layers which contain a minimum of defects and inhomogeneities. Success in minimizing dielectric defects and inhomogeneities means that one manufacturer's capacitors require less of a reduction in voltage rating than another with a less uniform and homogeneous dielectric of similar thickness does.

A second, equally important consideration regarding maximum useful voltage is the effect applied voltage stress has on the capacitance and dissipation factor of the MLC because of the ferroelectric properties of the dielectric. (Typically, Y5V, Z5U, and X7R dielectrics exhibit ferroelectricity; COG type dielectrics do not.)

Figure 1 shows graphically the percent change in capacitance from the zero field value at various voltage stress levels for three commercial Y5V capacitors from different manufacturers. The capacitors had dielectric thicknesses between 10 and 14µm and were rated for 16 volts. However, because of the thinness of their dielectrics, they exhibit useful ca-

capacitance only at significantly lower applied voltages:

Applied DC Voltage	Capacitance as a Percent of Zero Bias Value
0	100
3v	75-85
5v	48-62
12v	18-25
16v	10-15

Similarly, the 1kHz dissipation factor (d.f.) is quite dependent on voltage level. Figure 2 shows its dependence on A.C. signal level; Figure 3 shows the effect on d.f. of an imposed D.C. bias. A typical d.f. measurement at 0.5v RMS may provide little information about the capacitor's usefulness in a 5v D.C. application.

Lastly of course, ceramic dielectrics which provide the most capacitance (highest dielectric constants) also have the poorest temperature stability of capacitance. Figure 4 illustrates the relative capacitance and its temperature dependence for Y5V, Z5U, and X7R characteristic MLC capacitors. Usually the relative voltage stability of different dielectrics mirror their temperature stability.

Often Y5V characteristic ceramic dielectrics are combined with very thin dielectric layers to provide a maximum of capacitance in a small MLC. While these are useful devices, their rather substantial deviations from ideal capacitor behavior must be recognized and compensated for in their application.

Because of the complexity of the temperature and voltage dependencies of these capacitors, manufacturer catalog information is of only limited usefulness:

- Temperature characteristic designations are good indicators of electrical parameter changes with temperature.
- Rated voltages are good indicators of life test and surge voltage reliability.
- Rated voltages are not good indicators, manufacturer-to-manufacturer, of dielectric thickness because life test reliability depends strongly on the type and size of process-dependent imperfections in the dielectric.
- Rated voltages are probably good indicators of dielectric thickness for a single manufacturer.
- Rated voltages are not good indicators of electrical parameter performance at rated voltage.
- Capacitance values and tolerances may be very poor indicators of capacitance under use conditions.

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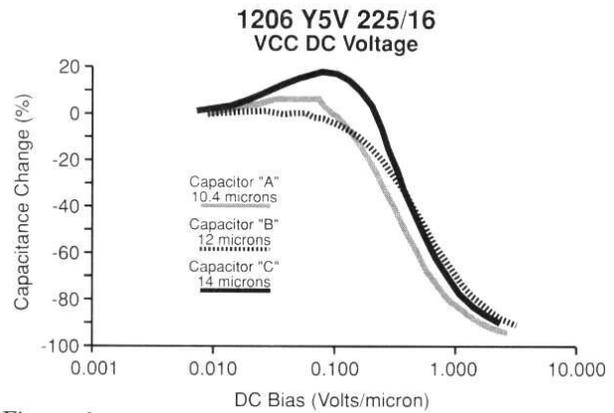


Figure 1

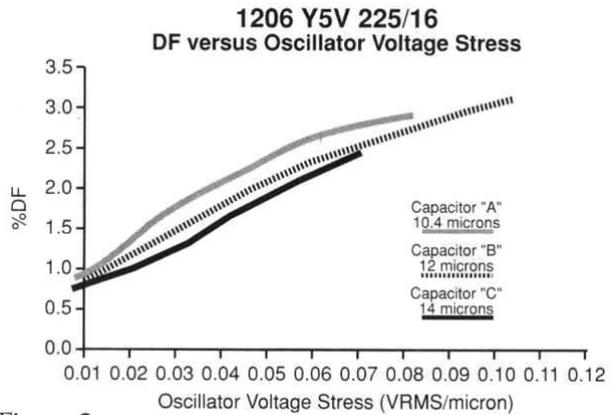


Figure 2

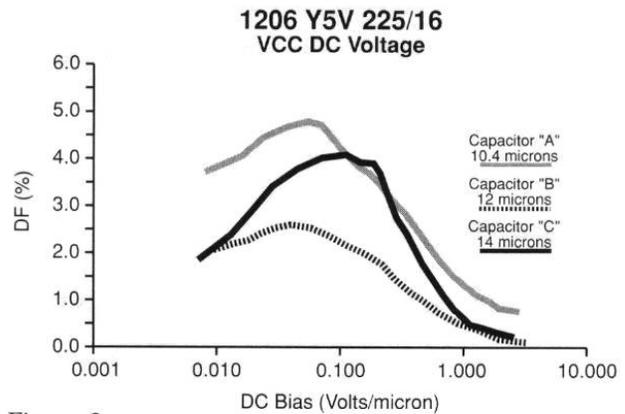


Figure 3

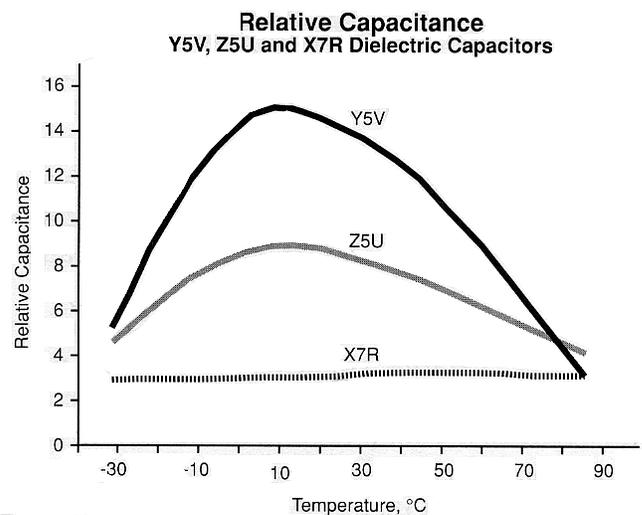


Figure 4