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T E C H T O P I C S

... *T H E L E A D I N G E D G E*

The technique of flex testing multilayer ceramic capacitor (MLC) chips, which was described in the September 1993 issue of Tech Topics, has generated much interest and several technical papers, including one chosen as a "best paper" at the 1994 Electronic Component and Technology Conference sponsored by the IEEE and EIA.

This edition of Tech Topics addresses a number of considerations in designing and conducting the test.

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Flex Testing II

by John Prymak

The purpose of the test is to generate variables information about the sensitivities of groups of MLC chips to damage from circuit board flexing. It is a test-to-failure technique.

In the test, a circuit board with a mounted ceramic capacitor is progressively bent as shown in Figure 1. The deflection of the board where the continuously monitored capacitance suddenly changes values characterizes the flex crack initiation of the chip.
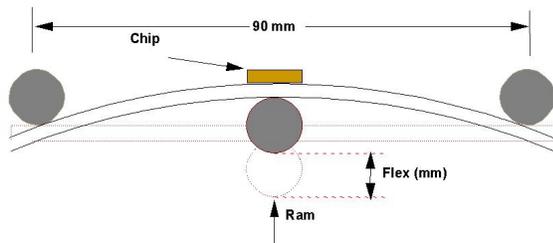

Figure 1. Flex Test with chip on top side - *normal* flex.

Reverse Flex

The arrangement in Figure 1 causes the chip to be on the convex side of the circuit board, so that the chip is effectively in tension. With sufficient flexure the chip will fail, usually with a characteristic crack traveling diagonally upward from the edge of the lower metal termination surface.

Chips have also been tested with the board reversed, so that the chip is on the concave side of the flexed board. A slot in the ram allows spacing between the ram and the chip, preventing physical contact between the two. In this test, the ram was driven to a flexure of 10mm, held for 2.5 seconds, then gradually withdrawn, as the data of Figure 2 represents. We also ran this test with an increase in the hold to 10 seconds as indicated in Figure 3. In every case the chip failed during the withdrawal of the ram and relaxation of flexure. With a 2.5 second dwell at the maximum flexure (Figure 2), the failure occurred at 6mm into the withdrawal. With the longer dwell, the failure occurred sooner, at 4mm into the withdrawal. Averages for 10 pieces tested in each condition were:

Condition	Distance to Failure
Reverse Flex (10mm), 2.5 sec. dwell	5.2mm from peak
Reverse Flex (10mm), 10 sec. dwell	4.7mm from peak
Normal Flex	4.4mm from start

Solder is a malleable metal. During the application of reverse flex, the chip is predominantly under compression (Figure 4). The compressive strength of ceramics is usually high, so that force will not damage the chip unless it has a substantial fault such as a delamination. The solder fillets, however, gradually deform outwardly to relieve the stress applied to them. When the board flexure is reduced, the partially deformed fillets cause the chip to experience increasing tensile stresses, and failure occurs in a similar manner and with a similar characteristic crack to that observed with normal flex testing. The longer the dwell at maximum flexure, the more stress-relieving deformation of the solder; hence, the earlier tensile stress builds on the chip during withdrawal of the ram.
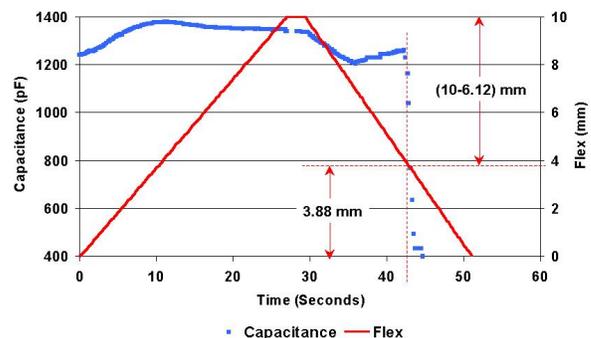

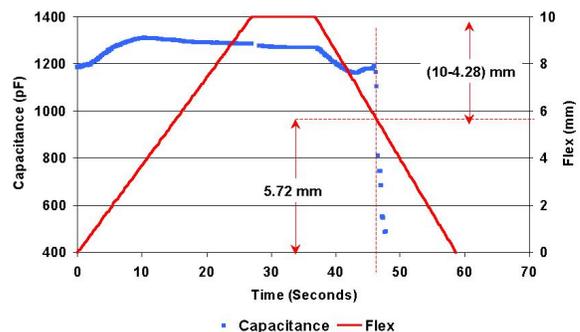**Figure 2. Reverse Flex with 2.5 Second Dwell.**

Figure 3. Reverse Flex with 10 Second Dwell.

It is unlikely that reverse flex testing will add chip-related information beyond that obtained with normal flex testing. However, the reverse flex test does illustrate the impact of solder properties on the flex test, and the need to conduct the test so as to minimize solder-related variation by considering:

a) amount of solder in the fillet,

b) composition/mechanical properties of the solder, and

c) rates of increase or decrease of stress on the solder joints.

It is now evident that the forces causing the crack in both the forward and reverse flex are the same - with the resulting cracks also the same. As such, visual examination cannot be used to determine in which direction the flexure was applied to cause a crack.
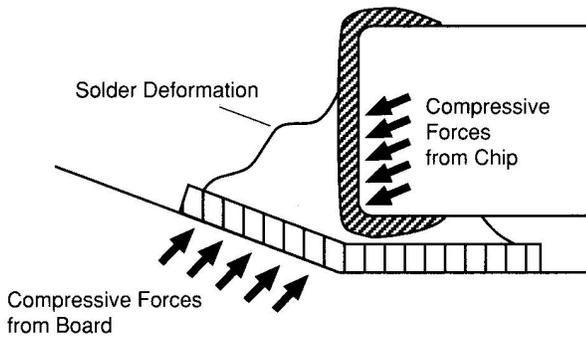

Figure 4. Solder Deformation on Reverse Flex

Mounting Considerations

The solder meniscus affects the amount of force transmitted to the component. Ideal solder fillets prescribed in testing for thermal crack robustness also apply to this test. Large amounts of solder will inhibit any movement within the solder and cause an earlier crack formation. The solder does move in a plastic state as the force is being applied. The release of some force, allowing a minor slippage, dissipates some of the force developing within the chip. Elimination or the reduction of this plastic movement through larger masses of solder would transmit higher stresses to the chip within a given flexure. The solder method should not factor the flex capability. If the solders are the same composition, there will be little difference in plastic deformation regardless of application method. Yet the application method may include another element into the force development. Glue adhesive used to hold the chip to the board during wave solder techniques will have such an effect.

For chips of smaller thickness (≤0.040 inches), this glue can act as a fulcrum in the center of the chip. Additional forces attempting to bend the chip over this fulcrum will act upon the chip. In cases such as this, it is not uncommon to see a chip cracked directly in the middle - removed from the termination areas where the typical flex crack is found. These cracks would appear as a typical mechanical crack.

If the chip is much thicker, the glue dot can have another effect. Since the force needed to crack a chip mechanically with this fulcrum model is inversely dependent upon the thickness, the thicker chip would withstand these forces to a higher degree. The glue can then act as a suppressant to board curvature beneath the chip, causing additional radiusing elsewhere, and moving the crack limit higher. The problem with these thicker chips in this wave solder application would be more thermal - as the ideal chip for thermal robustness is thinner.

Capacitance Monitoring Techniques

The capacitance monitoring has to be dynamic with the ram movement constant. If a pause is set up at specified flexures, such as at 0.5mm intervals, the solder movement will release the shear force as time increases. Given a long enough interval, the forces can come back to zero. The plastic deformation is minimized and controlled with reading as the unit is being continuously flexed at a consistent and reproducible rate.

Circuit Board Width

The 40mm width specified in EIA-J RC 3402 was found to be about the minimum to give consistent board bending results. Narrower boards exhibited variable bending characteristics and erratic test results due to weak spots in the epoxy-fiber composite boards. The flex results were higher with the narrower boards as the curvature was being absorbed at areas other than beneath the chip.

Sample Size

A very important part of the information generated by this test is the slope of the low-side tail of the distribution of flexure values. To provide some statistically meaningful information about the tail, a sample size of at least 32 is needed, and about 100 is preferable.

Ram Head Diameter

The ram which causes the board to flex has a head with a radius of 5mm. This is well below that necessary for an ideal board's curvature at 10mm, but considering that this is not an ideal board, there will be increased curvature beneath the chip, and reduced radius. All of our testing is on the same apparatus and using the same source of boards. If there are any acceleration factors resulting from this small radiused ram, then they apply equally to all devices that have been tested. Note that this is a substantially smaller radius ram than those specified in JIS C6429 and EIA-J RC 3402, both of which would exceed the radius of the circuit board in the range of flexures required to damage some chips.

Chip Size

When comparisons are made of the different chip sizes, the smaller size performs better. The difference in chip size causes different lengths between the terminations. With equal percentages of expansion for each size at any given flexure, the expansion length of the larger chip's termination separation causes a greater force to be applied to the chip.

We were able to test this comparison with one lot of units. By changing the amount of separation between the termination bands, we effectively mimicked the change in chip size. We split the lot into three groups. One was terminated in a well that was approximately 0.015" shallower than normal, one normal, and the last in a well that was approximately 0.015" deeper than normal. The well determines how much silver termination overlaps the sides of the chip (nominal for this chip is 0.020"). Figure 5 shows the result of this test for each margin.
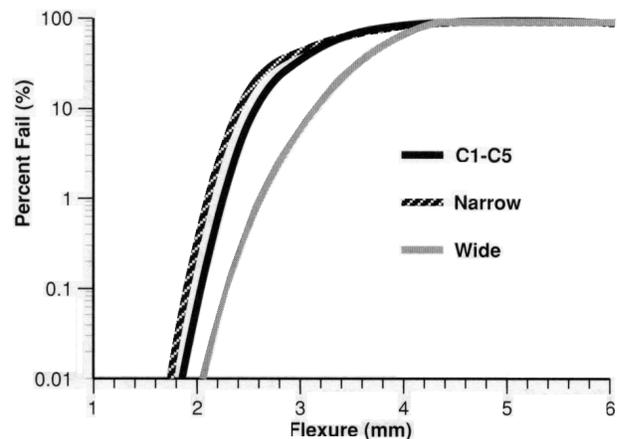

Figure 5. Simulation of Chip Size with Varied Silver Margins

The "deep" dip and wide termination bands reduce the length of exposed chip - duplicating the "smaller" chip size. These pieces flexed considerably higher than the "normal." There was not as much separation between the "normal" and the "shallow" dip (duplicating a larger than "normal" chip), but this may have been due to noise. It is easy to maintain a consistent deep dip; but with slight angles causing large discrepancies of margin overlap, the shallow dip may have been the most inconsistent.

Further information on this test and several groups of test results are contained in KEMET's technical publication F-2110 "Flex Testing With Capacitance Monitoring," by Jim Bergenthal and John Prymak. This bulletin will be available January 1995.

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