Multilayer ceramic capacitors are available in a variety of physical sizes and configurations, including leaded devices and surface mounted chips. Leaded styles include molded and conformally coated parts with axial and radial leads. However, the basic capacitor element is similar for all styles. It is called a chip and consists of formulated dielectric materials which have been cast into thin layers, interspersed with metal electrodes alternately exposed on opposite edges of the laminated structure. The entire structure is fired at high temperature to produce a monolithic block which provides high capacitance values in a small physical volume. After firing, conductive terminations are applied to opposite ends of the chip to make contact with the exposed electrodes. Termination materials and methods vary depending on the intended use.

TEMPERATURE CHARACTERISTICS

Ceramic dielectric materials can be formulated with a wide range of characteristics. The EIA standard for ceramic dielectric capacitors (RS-198) divides ceramic dielectrics into the following classes:

Class I: Temperature compensating capacitors, suitable for resonant circuit application or other applications where high Q and stability of capacitance characteristics are required. Class I capacitors have predictable temperature coefficients and are not affected by voltage, frequency or time. They are made from materials which are not ferro-electric, yielding superior stability but low volumetric efficiency. Class I capacitors are the most stable type available, but have the lowest volumetric efficiency.

Class II: Stable capacitors, suitable for bypass or coupling applications or frequency discriminating circuits where Q and stability of capacitance characteristics are not of major importance. Class II capacitors have temperature characteristics of ± 15% or less. They are made from materials which are ferro-electric, yielding higher volumetric efficiency but less stability. Class II capacitors are affected by temperature, voltage, frequency and time.

Class III: General purpose capacitors, suitable for by-pass coupling or other applications in which dielectric losses, high insulation resistance and stability of capacitance characteristics are of little or no importance. Class III capacitors are similar to Class II capacitors except for temperature characteristics, which are greater than ± 15%. Class III capacitors have the highest volumetric efficiency and poorest stability of any type.

KEMET leaded ceramic capacitors are offered in the three most popular temperature characteristics:

C0G: Class I, with a temperature coefficient of 0 ± 30 ppm per degree C over an operating temperature range of - 55°C to + 125°C (Also known as “NP0”).

X7R: Class II, with a maximum capacitance change of ± 15% over an operating temperature range of - 55°C to + 125°C.

Z5U: Class III, with a maximum capacitance change of + 22% - 56% over an operating temperature range of + 10°C to + 85°C.

Specified electrical limits for these three temperature characteristics are shown in Table 1.

SPECIFIED ELECTRICAL LIMITS

Parameter	Temperature Characteristics		
	C0G	X7R	Z5U
Dissipation Factor: Measured at following conditions. C0G – 1 kHz and 1 vrms if capacitance >1000pF 1 MHz and 1 vrms if capacitance ≤ 1000 pF X7R – 1 kHz and 1 vrms* or if extended cap range 0.5 vrms Z5U – 1 kHz and 0.5 vrms	0.10%	2.5% (3.5% @ 25V)	4.0%
Dielectric Stength: 2.5 times rated DC voltage.	Pass Subsequent IR Test		
Insulation Resistance (IR): At rated DC voltage, whichever of the two is smaller	1,000 MΩ–µF or 100 GΩ	1,000 MΩ–µF or 100 GΩ	1,000 MΩ–µF or 10 GΩ
Temperature Characteristics: Range, °C Capacitance Change without DC voltage	-55 to +125 0 ± 30 ppm/°C	-55 to +125 ± 15%	+ 10 to +85 +22%,-56%

* MHz and 1 vrms if capacitance ≤ 100 pF on military product.

Table I

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ELECTRICAL CHARACTERISTICS

The fundamental electrical properties of multilayer ceramic capacitors are as follows:

Polarity: Multilayer ceramic capacitors are not polar, and may be used with DC voltage applied in either direction.

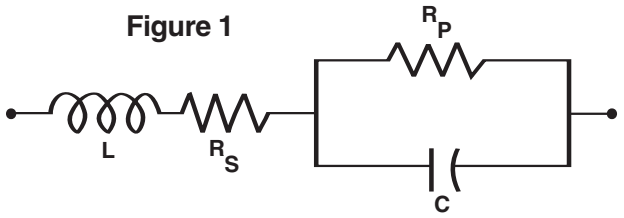
Rated Voltage: This term refers to the maximum continuous DC working voltage permissible across the entire operating temperature range. Multilayer ceramic capacitors are not extremely sensitive to voltage, and brief applications of voltage above rated will not result in immediate failure. However, reliability will be reduced by exposure to sustained voltages above rated.

Capacitance: The standard unit of capacitance is the farad. For practical capacitors, it is usually expressed in microfarads (10^{-6} farad), nanofarads (10^{-9} farad), or picofarads (10^{-12} farad). Standard measurement conditions are as follows:

Class I (up to 1,000 pF):	1MHz and 1.2 VRMS maximum.
Class I (over 1,000 pF):	1kHz and 1.2 VRMS maximum.
Class II:	1 kHz and 1.0 ± 0.2 VRMS.
Class III:	1 kHz and 0.5 ± 0.1 VRMS.

Like all other practical capacitors, multilayer ceramic capacitors also have resistance and inductance. A simplified schematic for the equivalent circuit is shown in Figure 1. Other significant electrical characteristics resulting from these additional properties are as follows:

Figure 1



C = Capacitance **R_S = Equivalent Series Resistance (ESR)**

L = Inductance **R_P = Insulation Resistance (IR)**

Impedance: Since the parallel resistance (Rp) is normally very high, the total impedance of the capacitor is:

$$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$$

Where **Z = Total Impedance**

RS = Equivalent Series Resistance

X_C = Capacitive Reactance = $\frac{1}{2\pi fC}$

X_L = Inductive Reactance = $2\pi fL$

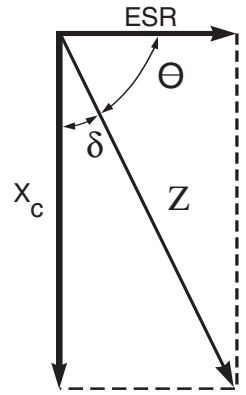
The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

Dissipation Factor: Dissipation Factor (DF) is a measure of the losses in a capacitor under AC application. It is the ratio of the equivalent series resistance to the capacitive reactance, and is usually expressed in percent. It is usually measured simultaneously with capacitance, and under the same conditions. The vector diagram in Figure 2 illustrates the relationship between DF, ESR, and impedance. The reciprocal of the dissipation factor is called the "Q", or quality factor. For convenience, the "Q" factor is often used for very low values of dissipation factor. DF is sometimes called the "loss tangent" or "tangent δ", as derived from this diagram.

Figure 2

$$DF = \frac{ESR}{X_C}$$

$$X_C = \frac{1}{2\pi fC}$$



Insulation Resistance: Insulation Resistance (IR) is the DC resistance measured across the terminals of a capacitor, represented by the parallel resistance (Rp) shown in Figure 1. For a given dielectric type, electrode area increases with capacitance, resulting in a decrease in the insulation resistance. Consequently, insulation resistance is usually specified as the "RC" (IR x C) product, in terms of ohm-farads or megohm-microfarads. The insulation resistance for a specific capacitance value is determined by dividing this product by the capacitance. However, as the nominal capacitance values become small, the insulation resistance calculated from the RC product reaches values which are impractical. Consequently, IR specifications usually include both a minimum RC product and a maximum limit on the IR calculated from that value. For example, a typical IR specification might read "1,000 megohm-microfarads or 100 gigohms, whichever is less."

Insulation Resistance is the measure of a capacitor to resist the flow of DC leakage current. It is sometimes referred to as "leakage resistance." The DC leakage current may be calculated by dividing the applied voltage by the insulation resistance (Ohm's Law).

Dielectric Withstanding Voltage: Dielectric withstanding voltage (DWV) is the peak voltage which a capacitor is designed to withstand for short periods of time without damage. All KEMET multilayer ceramic capacitors will withstand a test voltage of 2.5 x the rated voltage for 60 seconds.

KEMET specification limits for these characteristics at standard measurement conditions are shown in Table 1 on page 4. Variations in these properties caused by changing conditions of temperature, voltage, frequency, and time are covered in the following sections.

TABLE 1
EIA TEMPERATURE CHARACTERISTIC CODES FOR CLASS I DIELECTRICS

Significant Figure of Temperature Coefficient		Multiplier Applied to Temperature Coefficient		Tolerance of Temperature Coefficient *	
PPM per Degree C	Letter Symbol	Multi-plier	Number Symbol	PPM per Degree C	Letter Symbol
0.0	C	-1	0	±30	G
0.3	B	-10	1	±60	H
0.9	A	-100	2	±120	J
1.0	M	-1000	3	±250	K
1.5	P	-100000	4	±500	L
2.2	R	+1	5	±1000	M
3.3	S	+10	6	±2500	N
4.7	T	+100	7		
7.5	U	+1000	8		
		+10000	9		

** These symetrical tolerances apply to a two-point measurement of temperature coefficient: one at 25°C and one at 85°C. Some deviation is permitted at lower temperatures. For example, the PPM tolerance for C0G at -55°C is +30 / -72 PPM.*

TABLE 2
EIA TEMPERATURE CHARACTERISTIC CODES FOR CLASS II & III DIELECTRICS

Low Temperature Rating		High Temperature Rating		Maximum Capacitance Shift	
Degree Celcius	Letter Symbol	Degree Celcius	Number Symbol	Percent	Letter Symbol
+10C	Z	+45C	2	±1.0%	A
-30C	Y	+65C	4	±1.5%	B
-55C	X	+85C	5	±2.2%	C
		+105C	6	±3.3%	D
		+125C	7	±4.7%	E
		+150C	8	±7.5%	F
		+200C	9	±10.0%	P
				±15.0%	R
				±22.0%	S
				+22/-33%	T
				+22/-56%	U
				+22/-82%	V

EFFECT OF TEMPERATURE

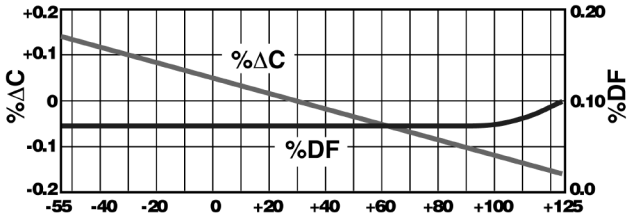


Figure 3. Temperature °C
Capacitance & DF vs Temperature - C0G

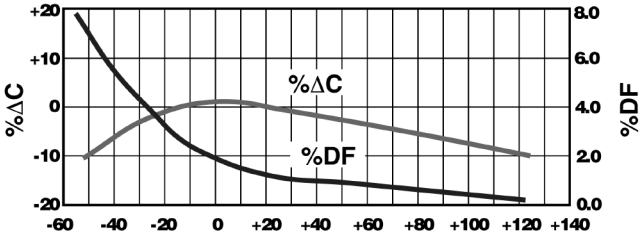


Figure 4. Temperature °C
Capacitance & DF vs Temperature - X7R

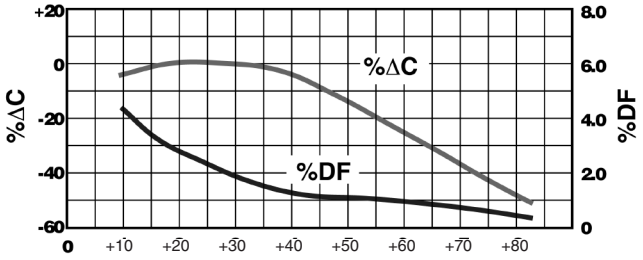


Figure 5. Temperature °C
Capacitance & DF vs Temperature - Z5U

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EFFECT OF APPLIED VOLTAGE

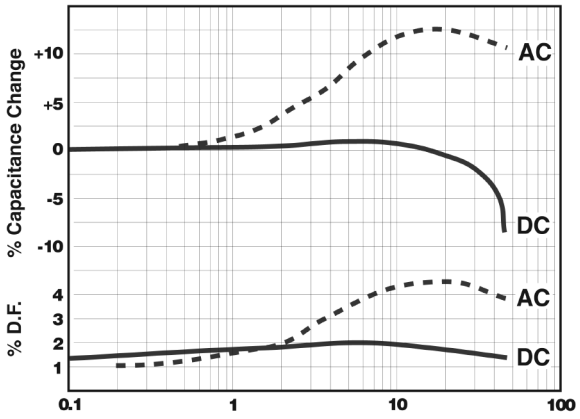

Figure 6. AC or DC Volts Applied
Typical Effects of 1000 Hz AC and DC Voltage Level on Capacitance and Dissipation Factor - X7R
Note: C0G Dielectric capacitance and dissipation factor are stable with voltage.

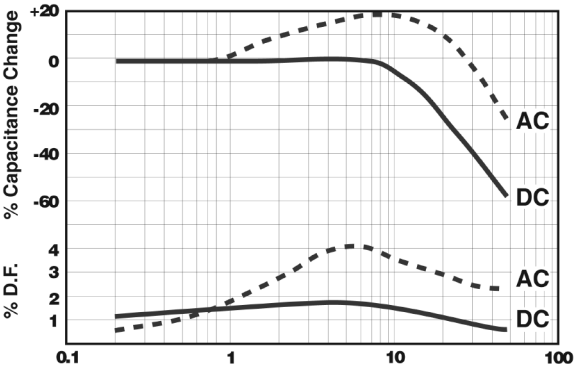

Figure 7. AC or DC Volts Applied
Typical Effects of 1000 Hz AC and DC Voltage Level on Capacitance and Dissipation Factor - Z5U
Note: C0G Dielectric capacitance and dissipation factor are stable with voltage.

Effect of Temperature: Both capacitance and dissipation factor are affected by variations in temperature. The maximum capacitance change with temperature is defined by the temperature characteristic. However, this only defines a "box" bounded by the upper and lower operating temperatures and the minimum and maximum capacitance values. Within this "box", the variation with temperature depends upon the specific dielectric formulation. Typical curves for KEMET capacitors are shown in Figures 3, 4, and 5. These figures also include the typical change in dissipation factor for KEMET capacitors.

Insulation resistance decreases with temperature. Typically, the insulation resistance at maximum rated temperature is 10% of the 25°C value.

Effect of Voltage: Class I ceramic capacitors are not affected by variations in applied AC or DC voltages. For Class II and III ceramic capacitors, variations in voltage affect only the capacitance and dissipation factor. The application of DC voltage higher than 5 vdc reduces both the capacitance and dissipation factor. The application of AC voltages up to 10-20 Vac tends to increase both capacitance and dissipation factor. At higher AC voltages, both capacitance and dissipation factor begin to decrease.

Typical curves showing the effect of applied AC and DC voltage are shown in Figure 6 for KEMET X7R capacitors and Figure 7 for KEMET Z5U capacitors.

Effect of Frequency: Frequency affects both capacitance and dissipation factor. Typical curves for KEMET multilayer ceramic capacitors are shown in Figures 8 and 9.

The variation of impedance with frequency is an important consideration in the application of multilayer ceramic capacitors. Total impedance of the capacitor is the vector of the capacitive reactance, the inductive reactance, and the ESR, as illustrated in Figure 2. As frequency increases, the capacitive reactance decreases. However, the series inductance (L) shown in Figure 1 produces inductive reactance, which increases with frequency. At some frequency, the impedance ceases to be capacitive and becomes inductive. This point, at the bottom of the V-shaped impedance versus frequency curves, is the self-resonant frequency. At the self-resonant frequency, the reactance is zero, and the impedance consists of the ESR only.

Typical impedance versus frequency curves for KEMET multilayer ceramic capacitors are shown in Figures 10, 11, and 12. These curves apply to KEMET capacitors in chip form, without leads. Lead configuration and lead length have a significant impact on the series inductance. The lead inductance is approximately 10nH/inch, which is large compared to the inductance of the chip. The effect of this additional inductance is a decrease in the self-resonant frequency, and an increase in impedance in the inductive region above the self-resonant frequency.

Effect of Time: The capacitance of Class II and III dielectrics change with time as well as with temperature, voltage and frequency. This change with time is known as "aging." It is caused by gradual realignment of the crystalline structure of the ceramic dielectric material as it is cooled below its Curie temperature, which produces a loss of capacitance with time. The aging process is predictable and follows a logarithmic decay. Typical aging rates for C0G, X7R, and Z5U dielectrics are as follows:

C0G	None
X7R	2.0% per decade of time
Z5U	5.0% per decade of time

Typical aging curves for X7R and Z5U dielectrics are shown in Figure 13.

The aging process is reversible. If the capacitor is heated to a temperature above its Curie point for some period of time, de-aging will occur and the capacitor will regain the capacitance lost during the aging process. The amount of de-aging depends on both the elevated temperature and the length of time at that temperature. Exposure to 150°C for one-half hour or 125°C for two hours is usually sufficient to return the capacitor to its initial value.

Because the capacitance changes rapidly immediately after de-aging, capacitance measurements are usually delayed for at least 10 hours after the de-aging process, which is often referred to as the "last heat." In addition, manufacturers utilize the aging rates to set factory test limits which will bring the capacitance within the specified tolerance at some future time, to allow for customer receipt and use. Typically, the test limits are adjusted so that the capacitance will be within the specified tolerance after either 1,000 hours or 100 days, depending on the manufacturer and the product type.

POWER DISSIPATION

Power dissipation has been empirically determined for two representative KEMET series: C052 and C062. Power dissipation capability for various mounting configurations is shown in Table 3. This table was extracted from Engineering Bulletin F-2013, which provides a more detailed treatment of this subject.

Note that no significant difference was detected between the two sizes in spite of a 2 to 1 surface area ratio. Due to the materials used in the construction of multilayer ceramic capacitors, the power dissipation capability does not depend greatly on the surface area of the capacitor body, but rather on how well heat is conducted out of the capacitor lead wires. Consequently, this power dissipation capability is applicable to other leaded multilayer styles and sizes.

TABLE 3
POWER DISSIPATION CAPABILITY
(Rise in Celsius degrees per Watt)

Mounting Configuration	Power Dissipation of C052 & C062
1.00" leadwires attached to binding post of GR-1615 bridge (excellent heat sink)	90 Celsius degrees rise per Watt ±10%
0.25" leadwires attached to binding post of GR-1615 bridge	55 Celsius degrees rise per Watt ±10%
Capacitor mounted flush to 0.062" glass-epoxy circuit board with small copper traces	77 Celsius degrees rise per Watt ±10%
Capacitor mounted flush to 0.062" glass-epoxy circuit board with four square inches of copper land area as a heat sink	53 Celsius degrees rise per Watt ±10%

As shown in Table 3, the power dissipation capability of the capacitor is very sensitive to the details of its use environment. The temperature rise due to power dissipation should not exceed 20°C. Using that constraint, the maximum permissible power dissipation may be calculated from the data provided in Table 3.

It is often convenient to translate power dissipation capability into a permissible AC voltage rating. Assuming a sinusoidal wave form, the RMS "ripple voltage" may be calculated from the following formula:

$$E = Z \times \sqrt{\frac{P_{MAX}}{R}}$$

Where E = RMS Ripple Voltage (volts)

P = Power Dissipation (watts)

Z = Impedance

R = ESR

The data necessary to make this calculation is included in Engineering Bulletin F-2013. However, the following criteria must be observed:

1. The temperature rise due to power dissipation should be limited to 20°C.
2. The peak AC voltage plus the DC voltage must not exceed the maximum working voltage of the capacitor.

Provided that these criteria are met, multilayer ceramic capacitors may be operated with AC voltage applied without need for DC bias.

RELIABILITY

A well constructed multilayer ceramic capacitor is extremely reliable and, for all practical purposes, has an infinite life span when used within the maximum voltage and temperature ratings. Capacitor failure may be induced by sustained operation at voltages that exceed the rated DC voltage, voltage spikes or transients that exceed the dielectric withstanding voltage, sustained operation at temperatures above the maximum rated temperature, or the excessive temperature rise due to power dissipation.

Failure rate is usually expressed in terms of percent per 1,000 hours or in FITS (failure per billion hours). Some KEMET series are qualified under U.S. military established reliability specifications MIL-PRF-20, MIL-PRF-123, MIL-PRF-39014, and MIL-PRF-55681. Failure rates as low as 0.001% per 1,000 hours are available for all capacitance / voltage ratings covered by these specifications. These specifications and accompanying Qualified Products List should be consulted for details.

For series not covered by these military specifications, an internal testing program is maintained by KEMET Quality Assurance. Samples from each week's production are subjected to a 2,000 hour accelerated life test at 2 x rated voltage and maximum rated temperature. Based on the results of these tests, the average failure rate for all non-military series covered by this test program is currently 0.06% per 1,000 hours at maximum rated conditions. The failure rate would be much lower at typical use conditions. For example, using MIL-HDBK-217D this failure rate translates to 0.9 FITS at 50% rated voltage and 50°C.

Current failure rate details for specific KEMET multilayer ceramic capacitor series are available on request.

MISAPPLICATION

Ceramic capacitors, like any other capacitors, may fail if they are misapplied. Typical misapplications include exposure to excessive voltage, current or temperature. If the dielectric layer of the capacitor is damaged by misapplication the electrical energy of the circuit can be released as heat, which may damage the circuit board and other components as well.

If potential for misapplication exists, it is recommended that precautions be taken to protect personnel and equipment during initial application of voltage. Commonly used precautions include shielding of personnel and sensing for excessive power drain during board testing.

STORAGE AND HANDLING

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp, and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40° C, and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts, and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability, chip stock should be used promptly, preferably within 1.5 years of receipt.

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EFFECT OF FREQUENCY

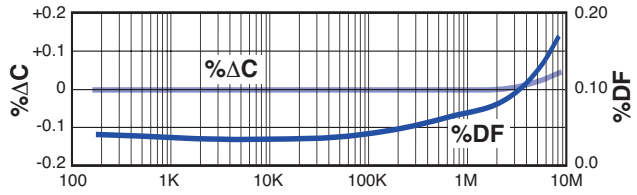

Figure 8. Frequency - Hertz
Capacitance & DF vs Frequency - C0G

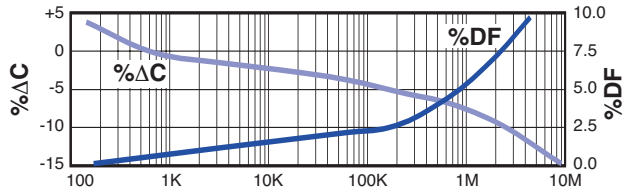

Figure 9. Frequency - Hertz
Capacitance & DF vs Frequency - X7R & Z5U

EFFECT OF TIME (hours)

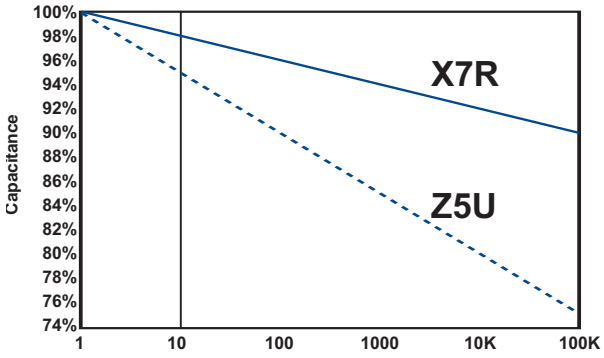

Figure 13. Typical Aging Rates for X7R & Z5U

IMPEDANCE VS FREQUENCY

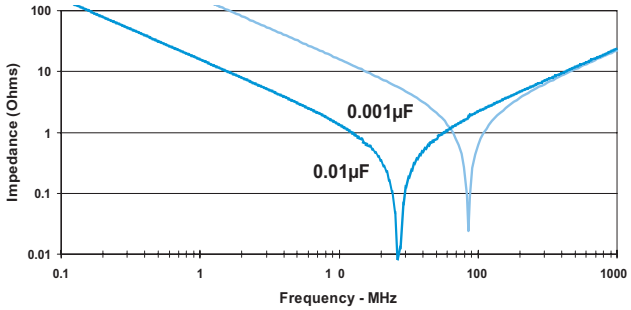

Figure 10. Impedance vs Frequency for C0G Dielectric

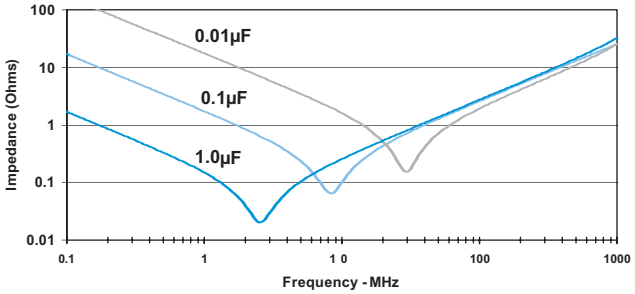

Figure 11. Impedance vs Frequency for X7R Dielectric

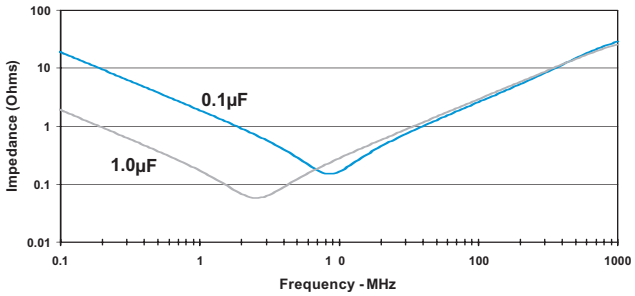

Figure 12. Impedance vs Frequency for Z5U Dielectric