

Introduction

Improving the volumetric efficiency of ceramic capacitors (capacitance per unit volume) is essential if the trends of increasing functionality and decreasing size and cost of electronic systems is to continue. Increasing volumetric efficiency allows designers to use smaller components for the same capacitance value (for instance, replacing an 0805 0.1 μF with an 0603 0.1 μF chip). It also leads to the availability of ceramic capacitors with increasing capacitance values in each chip size, providing designers with options to use ceramic capacitors in applications that have traditionally utilized tantalum capacitors (for instance, replacing a 1 μF tantalum with a 1 μF ceramic). The following article, written by March Maguire and Christos Kyriacou, describes the approach that KEMET has taken to develop a manufacturing platform that allows significant improvement in the volumetric efficiency of its multilayer ceramic capacitor product line. The simultaneous development of manufacturing and materials platforms (which will be described in a later issue of KEMET Tech Topics) is providing a foundation for the introduction of product families with volumetric efficiencies that are 1-2 orders of magnitude higher than those that are available today.

Dr. Larry A. Mann
Director, Ceramic Technology Development

Manufacturing of High Capacitance Value MLCC

by Christos Kyriacou and March Maguire

An important driver in the electronics industry is improved volumetric efficiency. KEMET remains committed to providing its customers with ceramic and tantalum capacitors that allow them to stay on the leading edge of this technological trend. With regard to Multilayer Ceramic Capacitors (MLCC), increasing volumetric efficiency requires manufacturing ceramic chips with larger numbers of thinner dielectric layers. Every 50% reduction in dielectric thickness results in a 400% increase in volumetric efficiency (the capacitance of each layer doubles, and twice as many layers will fit in a given size chip; hence the fourfold increase in capacitance). Today, the most popular MLCCs have dielectric thicknesses of about 8-10 microns, and have a maximum voltage rating of 25v. This is about half the dielectric thickness of a typical MLCC just a few years ago, which came with 50v ratings. MLCC with a 10v rating are already available from KEMET with 5-6 micron dielectric thicknesses. Typical dielectric thicknesses will continue to decline, approaching 1-2 micron, and be accompanied by a 3v rating before the year 2000. Maintaining the high quality and excellent reliability expected of MLCC presents

significant process, material, and equipment challenges as the active layers become thinner and the number of active layers increases. KEMET has developed and implemented into high-volume production a process that meets these challenges head on. This process is called the KEMET Tape Process, or KTP.

Today, the KTP is being used to manufacture high quality, high reliability MLCC with more than 150 active layers, each 5-6 microns thick (for example, an 0805 1.0 μF 10v rated X7R). In KEMET's Ceramic Technology Center, the capabilities of the KTP are being further enhanced, providing the capability to manufacture MLCC with more than 500 layers, each 2-3 microns thick. Achieving these capabilities requires new levels of precision and control, along with a new class of materials and handling techniques.

Preparation of the Dielectric Layers

The KTP is based on providing a high-quality green (unfired) ceramic coating on a polymer carrier film. The carrier film provides support that ensures that ultra-thin ceramic layers can be processed without being damaged. The thickness and quality of the green ceramic coatings are critical in determining the quality and reliability of the MLCC, with regard to both their physical characteristics and electrical properties. Dielectric thickness must be controlled to within 0.25 microns to maintain chip dimensions and capacitance targeting. Anomalies in the coating (pinholes, voids, contamination) which might be benign in a 15 μm dielectric are potentially catastrophic in a 5 μm dielectric, and therefore must be eliminated. The coating method, the ceramic particle size distribution, and the formulation of the ceramic and organic mixture have all been selected to ensure that the uniformity and quality of the finished dielectric film meet KEMET's stringent requirements. The ceramic slurry/slip undergo special processing in order to prevent agglomeration of the binders and ceramic particles. The dielectric and organic formulation is optimized to provide the necessary wetting properties to coat the carrier film, and the proper chemistry to guarantee release from the carrier film during subsequent processing.

KEMET evaluated several coating methods, and chose a method that not only ensures high quality dielectric films even in layers approaching 1 micron in thickness, but one that is also able to operate at high speed (10-30 meters per minute), thus providing an economical process that is capable of meeting the needs of high-volume manufacturing. KEMET has been able to accomplish this without resorting to the use of organic solvent systems commonly used by other MLCC manufacturers. Instead, the KTP continues KEMET's tradition of utilizing environmentally friendly water-based binder systems for manufacturing the ceramic dielectric layers.

Processing of Individual Layers into MLCC

KEMET has developed a unique process to manufacture MLCC with extremely thin layers while maintaining excellent product quality. The process involves printing a pattern of thin, uniform electrodes on the ceramic film while the ceramic is still supported by the carrier film. The printed layers are then lifted off the carrier film and laminated together into a pad containing thousands of individual MLCC using a highly automated system. A high-speed image processing system is used to align each layer, enabling the entire system to run at speeds exceeding a layer every 2 seconds. Dielectric layers as thin as 2 microns have been successfully processed, and indications are that with further improvements, processing of 1 micron layers will be possible. Currently, high volume prototype samples are being made with 3.5 micron thick layers. The details of this process are proprietary, but examples of products being manufactured include 4.7 and 10 μF 1206 MLCC with both X7R and Y5V characteristics.

Electrode thickness, uniformity, and quality are also important factors in building MLCC with large numbers of thin ceramic layers. This subject was discussed in some detail in the June 1997 issue of KEMET Tech Topics. Electrodes in MLCC with 2-3 micron thick dielectric layers must be free of lumps that might "punch through" the dielectric layer, creating a short, and should be as thin as possible to minimize stresses between the ceramic and electrode layers while maintaining high conductivity to minimize DF and ESR. As part of the KTP program, new equipment, processes, and materials have been introduced in KEMET's electrode paste manufacturing facilities. These improvements have resulted in a reduction of 30-50% in electrode thickness while improving electrode uniformity.

Turning Capabilities into Products

The KEMET Tape Process, combined with the development of ultra-fine grained ceramic dielectrics (to be discussed in an upcoming issue of KEMET Tech Topics), is allowing KEMET to begin manufacture of products with volumetric efficiencies that were unimaginable just a few years ago. This photograph shows a partial cross section of an 11 μF 1206 MLCC with X7R characteristics that contains 440 dielectric layers, each 3 microns thick. Just one example of the products that KEMET is producing in its Ceramic Technology Development Center. This and similar products will be introduced into high-volume manufacture during the coming months.

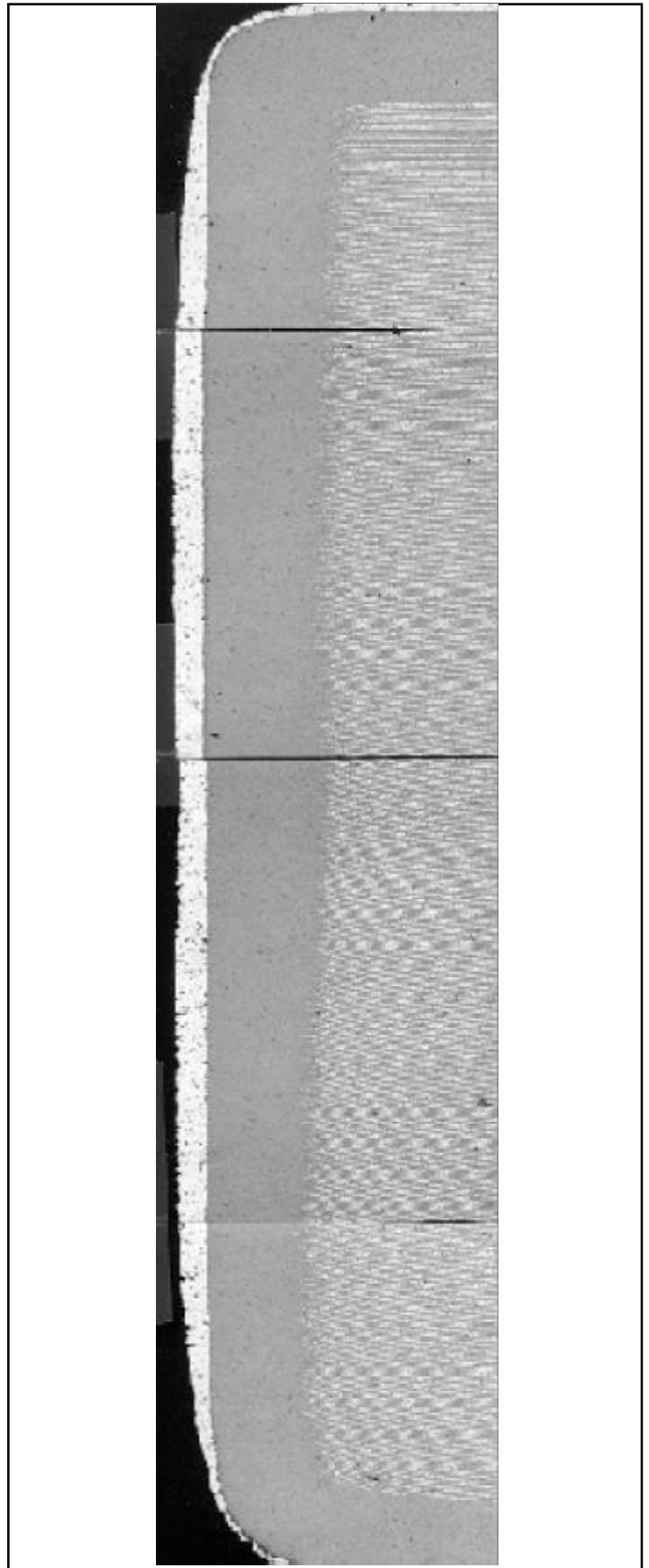


Figure 1. Partial cross section of an 11 μF , 1206, MLCC - X7R, 440 dielectric layers, 3 microns thick

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